

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING NATIONAL PHASE OF
PCT APPLICATION UNDER 35 U.S.C. 371 AND 37 CFR 1.494 OR 1.495

09/830361

To: Hon. Commissioner of Patents
Washington, D.C. 20231



00909

TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)

Atty Dkt: P 279059 /7049P-U
M# /Client Ref.

From: Pillsbury Winthrop LLP, IP Group:

Date: April 25, 2001

This is a **REQUEST** for **FILING** a PCT/USA National Phase Application based on:

- | | | |
|--|--|--|
| 1. International Application

PCT/JP00/05972
↑ country code | 2. International Filing Date

1 September 2000
Day MONTH Year | 3. Earliest Priority Date Claimed

2 September 1999
Day MONTH Year
(use item 2 if no earlier priority) |
|--|--|--|
4. Measured from the earliest priority date in item 3, this PCT/USA National Phase Application Request is being filed within:

(a) ☒ 20 months from above item 3 date (b) ☐ 30 months from above item 3 date,

(c) Therefore, the due date (unextendable) is May 2, 2001
5. Title of Invention PRINTED CIRCUIT BOARD AND METHOD FOR MANUFACTURING PRINTED CIRCUIT BOARD
6. Inventor(s) INAGAKI, Yasushi et al

Applicant herewith submits the following under 35 U.S.C. 371 to effect filing:

7. ☒ Please immediately start national examination procedures (35 U.S.C. 371 (f)).
8. ☐ A copy of the International Application as filed (35 U.S.C. 371(c)(2)) is transmitted herewith (file if in English but, if in foreign language, file only if not transmitted to PTO by the International Bureau) including:
- a. ☐ Request;
 - b. ☐ Abstract;
 - c. _____ pgs. Spec. and Claims;
 - d. _____ sheet(s) Drawing which are ☐ informal ☐ formal of size ☐ A4 ☐ 11"
9. ☒ A copy of the International Application has been transmitted by the International Bureau.
10. A translation of the International Application into English (35 U.S.C. 371(c)(2))
- a. ☒ is transmitted herewith including: (1) ☐ Request; (2) ☒ Abstract;
(3) 163 pgs. Spec. and Claims;
(4) 73 sheet(s) Drawing which are:
☐ informal ☒ formal of size ☒ A4 ☐ 11"
 - b. ☐ is not required, as the application was filed in English.
 - c. ☐ is not herewith, but will be filed when required by the forthcoming PTO Missing Requirements Notice per Rule 494(c) if box 4(a) is X'd or Rule 495(c) if box 4(b) is X'd.
 - d. ☐ Translation verification attached (not required now).

RE: USA National Phase Filing of PCT /JP00/05972

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11. ☒ Please see the attached Preliminary Amendment
12. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)), i.e., before 18th month from first priority date above in item 3, are transmitted herewith (file only if in English) including:
13. ☒ PCT Article 19 claim amendments (if any) have been transmitted by the International Bureau
14. ☐ Translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)), i.e., of **claim amendments** made before 18th month, is attached (required by 20th month from the date in item 3 if box 4(a) above is X'd, or 30th month if box 4(b) is X'd, or else amendments will be considered canceled).
15. **A declaration of the inventor** (35 U.S.C. 371(c)(4))
 a. ☒ is submitted herewith ☒ Original ☐ Facsimile/Copy
 b. ☐ is not herewith, but will be filed when required by the forthcoming PTO Missing Requirements Notice per Rule 494(c) if box 4(a) is X'd or Rule 495(c) if box 4(b) is X'd.
16. **An International Search Report (ISR):**
 a. Was prepared by ☐ European Patent Office ☒ Japanese Patent Office ☐ Other
 b. ☒ has been transmitted by the international Bureau to PTO.
 c. ☒ copy herewith (2 pg(s).) ☒ plus Annex of family members (1 pg(s).).
17. **International Preliminary Examination Report (IPER):**
 a. ☒ has been transmitted (if this letter is filed after 28 months from date in item 3) in English by the International Bureau with Annexes (if any) in original language.
 b. ☐ copy herewith in English.
 c.1 ☐ IPER Annex(es) in original language ("Annexes" are amendments made to claims/spec/drawings during Examination) including attached amended:
 c.2 ☐ Specification/claim pages # _____ claims # _____
 Dwg Sheets # _____
 d. ☐ Translation of Annex(es) to IPER (required by 30th month due date, or else annexed amendments will be considered canceled).
18. **Information Disclosure Statement** including:
 a. ☒ Attached Form PTO-1449 listing documents
 b. ☒ Attached copies of documents listed on Form PTO-1449
 c. ☒ A concise explanation of relevance of ISR references is given in the ISR.
19. ☒ **Assignment** document and Cover Sheet for recording are attached. Please mail the recorded assignment document back to the person whose signature, name and address appear at the end of this letter.
20. ☐ Copy of Power to IA agent.
21. ☐ **Drawings** (complete only if 8d or 10a(4) not completed): _____ sheet(s) per set: ☐ 1 set informal;
☐ Formal of size ☐ A4 ☐ 11"
22. Small Entity Status ☒ is **Not** claimed ☐ is claimed (pre-filing confirmation required)
 22(a) _____ (No.) Small Entity Statement(s) enclosed (since 9/8/00 Small Entity Statements(s) not essential to make claim)
23. **Priority** is hereby claimed under 35 U.S.C. 119/365 based on the priority claim and the certified copy, both filed in the International Application during the international stage based on the filing in (country) JAPAN of:
- | | <u>Application No.</u> | <u>Filing Date</u> | | <u>Application No.</u> | <u>Filing Date</u> |
|-----|------------------------|--------------------|-----|------------------------|--------------------|
| (1) | 11-248311 | Sept. 2, 1999 | (2) | 11-360306 | Dec. 20, 1999 |
| (3) | 2000-103730 | April 5, 2000 | (4) | 2000-103731 | April 5, 2000 |
| (5) | 2000-103732 | April 5, 2000 | (6) | 2000-103733 | April 5, 2000 |
- a. ☒ See Form PCT/IB/304 sent to US/DO with copy of priority documents. If copy has not been received, please proceed promptly to obtain same from the IB.
- b. ☒ Copy of Form PCT/IB/304 attached.

24. Attached:

JCO8 Rec'd PCT/PTO 25 APR 2007

25 Per Item 17.c2, **cancel original** pages #_____, claims #_____, Drawing Sheets #**26. Calculation of the U.S. National Fee (35 U.S.C. 371 (c)(1)) and other fees is as follows:**Based on amended claim(s) per above item(s) ☐ 12, ☐ 14, ☐ 17, ☐ 25 (hilitte)

Total Effective Claims	97	minus 20 =	77	x \$18/\$9	=	\$1386	966/967
Independent Claims	17	minus 3 =	14	x \$80/\$40	=	\$1120	964/965
If any proper (ignore improper) Multiple Dependent claim is present,				add\$270/\$135	+	270	968/969

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(4)): →→ **BASIC FEE REQUIRED, NOW** →→→→A. If country code letters in item 1 are not "US", "BR", "BB", "TT", "MX", "IL", "NZ", "IN" or "ZA"

See item 16 re:

1. Search Report was <u>not</u> prepared by EPO or JPO -----	add\$1000/\$500	960/961
2. Search Report was prepared by EPO or JPO -----	add\$860/\$430	970/971
	<u>+860</u>	

SKIP B, C, D AND E UNLESS country code letters in item 1 are "US", "BR", "BB", "TT", "MX", "IL", "NZ", "IN" or "ZA"

(X) → <input type="checkbox"/> B. If <u>USPTO</u> did not issue <u>both</u> International Search Report (ISR) and (if box 4(b) above is X'd) the International Examination Report (IPER), -----	add\$1000/\$500	+0	960/961
(only) → <input type="checkbox"/> C. If <u>USPTO</u> issued ISR but not IPER (or box 4(a) above is (one) X'd), -----	add\$710/\$355	+0	958/959
(off) → <input type="checkbox"/> D. If <u>USPTO</u> issued IPER but IPER Sec. V boxes <u>not</u> all 3 (these) YES, -----	add\$690/\$345	+0	956/957
(4) → <input type="checkbox"/> E. If international preliminary examination fee was paid to (boxes) <u>USPTO</u> and Rules 492(a)(4) and 496(b) <u>satisfied</u> (IPER Sec. V <u>all</u> 3 boxes YES for <u>all</u> claims), -----	add \$100/\$50	+0	962/963
SUBTOTAL =		\$3636	

28. If Assignment box 19 above is X'd, add Assignment Recording fee of ---\$40 +40 (581)

29. Attached is a check to cover the ----- **TOTAL FEES** \$3676

Our Deposit Account No. 03-3975

Our Order No. 41226 279059

C#

M#



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CHARGE STATEMENT: The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 and 492 (missing or insufficient fee only) now or hereafter relative to this application and the resulting Official document under Rule 20, or credit any overpayment, to our Account/Order Nos. shown above for which purpose a duplicate copy of this sheet is attached.

This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed

Pillsbury Winthrop LLP
Intellectual Property Group

By Atty: Glenn J. PerryReg. No. 28458Sig: [Signature]

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Atty/Sec: gjp/mhn

NOTE: File in duplicate with 2 postcard receipts (PAT-103) & attachments.

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25 APR 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION OF

Inventor(s): INAGAKI, Yasushi et al

Filed: Herewith

Title: PRINTED CIRCUIT BOARD AND METHOD FOR MANUFACTURING PRINTED
CIRCUIT BOARD

April 25, 2001

PRELIMINARY AMENDMENTHon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Please amend this application as follows:

IN THE SPECIFICATION:

At the top of the first page, just under the title, insert

☒ --This application is the National Phase of International Application
PCT/JP00/05972 filed September 1, 2000 which designated the U.S.
and that International Application☐ was ☒ was not published under PCT Article 21(2) in English.--

Respectfully submitted,

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SCANNED # 8

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SPECIFICATION

PRINTED CIRCUIT BOARD AND METHOD FOR MANUFACTURING PRINTED CIRCUIT BOARD

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Technical Field

The present invention relates to a printed circuit board on which electric elements, such as IC chips, are mounted. More specifically, the present invention
10 relates to a printed circuit board incorporating capacitors therein, and a method for manufacturing the same.

Background Art

15 In a computer, the length of electric wiring between the power supply and the IC chip is usually long, and therefore, the loop inductance at this electric wiring is extremely large. The variation in the voltage at which the IC is driven in high-speed operation mode
20 becomes very large accordingly, possibly causing malfunction of the IC. In addition, it becomes difficult to stabilize the voltage of the power supply. In an attempt to avoid these troubles, a capacitor is mounted on the surface of the printed circuit board as an auxiliary
25 device for assisting the power supply operation.

Specifically, the loop inductance which causes the variation in voltage depends on the length of electric wire from a power supply shown in Fig. 72(A) to a power supply terminal 272P of an IC chip 270 through a power
30 supply line in a printed circuit board 300, and the length of electric wire from a ground terminal 272E in the IC chip 270 to the power supply through a ground line in the printed circuit board 300 from the power supply. The

loop inductance can be reduced by narrowing the distance between the electric wires through which a current in a reverse direction to each other flows, for example, the distance between the power supply line and the ground line.

Therefore, as shown in Fig. 72(B), a chip capacitor 298 is mounted on the surface of the printed circuit board 300, thereby shortening the length of electric wire between the power supply line and the ground line in the printed circuit board 300 which connects the IC chip 270 to the chip capacitor 292 to be the power supply source, as well as narrowing the distance between the electric wires.

However, the degree of the voltage drop, which causes the variation in the IC driving voltage, depends on the frequency at which the IC chip is driven. As the frequency at which the IC chip is driven increases, it becomes impossible to reduce the loop inductance even if the chip capacitor is mounted on the surface of the printed circuit board 300 as is conducted in the case shown in Fig. 72(B). As a result, it becomes difficult to sufficiently suppress the variation in the IC driving voltage.

In this situation, the present inventors have conceived to mount a chip capacitor inside the printed circuit board. As a method for embedding a capacitor into a substrate, techniques described in Japanese Unexamined Patent Publications Nos. 6-326472, 7-263619, 10-256429, 11-45955, 11-126978, 11-312868 and the like may be employed.

Japanese Unexamined Patent Publication 6-326472 discloses a technique in which a capacitor is embedded in a substrate made of resin such as glass epoxy. This

structure reduces the noise in the power supply, and eliminates the need of the space for mounting the chip capacitor, thereby reducing the size of insulating substrate. Japanese Unexamined Patent Publication No. 7-263619 discloses a technique in which a capacitor is embedded into to a substrate made of ceramics or alumina. The capacitor is connected between the power supply layer and the ground layer. This structure shortens the length of electric wire and reduces the inductance of the electric wire.

However, these prior art techniques described above cannot satisfactorily shorten the distance between the IC chip and the capacitor, and also cannot reduce the inductance at the higher frequency domain of the IC chip to a level required at present. In particularly, a buildup multi-layer printed circuit board made of resin has problems such as disconnection between the terminal of the chip capacitor and the via hole, the peeling of the chip capacitor from the interlayer resin insulating layer, and the generation of cracks in the interlayer resin insulating layer, resulted from the difference in thermal expansion coefficients between the capacitor made of ceramics, and the core substrate and the interlayer resin insulating layer made of resin. These problems hinder the printed circuit board from having high reliability over a long period of time.

The present invention has been made to solve the above-described problems of the prior arts, and the objective thereof is to provide a printed circuit board capable of reducing a loop inductance and having high reliability, and a method for manufacturing the same.

Disclosure of the Invention

In order to achieve the above purpose, according to claim 1, a printed circuit board is characterized by comprising a core substrate, and a resin insulating layer and a conductor circuit laminated on the core substrate, wherein a cavity is formed in the core substrate, and a plurality of capacitors are accommodated in the cavity.

In the invention recited in claim 1, a large cavity is formed in a core substrate, and a plurality of capacitors are accommodated in the cavity. With this arrangement, a plurality of capacitors can be reliably provided within the core substrate. The capacitors can be provided at places close to each other in the cavity, the package density of the capacitors can be increased. Since a plurality of capacitors are mounted within the cavity, the plurality of capacitors are aligned to the same heights with each other. A resin layer can be formed on the core substrate into a uniform thickness, and via holes can be stably formed. Since the cavity is formed in such a manner as to have a large area, the capacitors can be provided at accurate positions. As a result, an interlayer resin insulating layer and a conductor circuit can be properly formed on the core substrate, thereby lowering the rate of generating defective printed circuit boards.

The cavity is preferably filled with a resin. The resin eliminates a space between the capacitors and the core substrate. As a result, the behavior of the capacitors incorporated in the core substrate becomes small. In addition, even if the stress is generated caused by the capacitors, the stress can be alleviated by the resin charged in the space. The resin also has an effect of adhering the capacitors to the core substrate, and lowering a migration between the capacitors and the

core substrate.

In the invention recited in claim 2, a resin is charged between the capacitors in the cavity. With this arrangement, the capacitors can be fixed in the cavity after deciding their positions in the capacitors. The thermal expansion coefficient of the resin is made to be smaller than a thermal expansion coefficient of the core substrate, that is, is set to the value close to that of the chip capacitor made of ceramics. In this manner, even if internal stress is generated between the core substrate and the capacitors caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur in the core substrate. As a result, high reliability can be attained. In addition, no migration is generated, and the connection with the capacitors is stabilized.

In the invention recited in claim 3, a through hole is formed between the capacitors in the resin layer, and a signal line does not pass through the chip capacitors. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body.

The through holes enable the establishment of an electric connection between the front surface and the back surface of the printed circuit board. In addition, a wire can be provided below the capacitors through the buildup layer, and pins and BGAs for the capacitors can be provided.

In the invention recited in claim 4, an electric connection for electrodes formed with a metal film of the capacitors is established by via holes formed by plating. The electrodes of the chip capacitor are made

by metallizing, and have pits and projections on their surfaces. However, the surfaces become smooth by formation of the metal film, and the via holes are then formed on the smooth surfaces. In this manner, when penetrating openings are formed in the resin coating the electrodes, no resin remains, and a reliability of the connection between the via holes and the electrodes can be increased. Furthermore, since the via holes are made by plating into the electrodes formed with the copper plated film, the electrodes are firmly connected to the via holes. No disconnection occurs between the electrodes and via holes even when a heat cycle test is conducted.

The metal film formed on the electrodes of the capacitors preferably includes any one of metals selected from the group consisting of copper, nickel, and noble metals. Tins and zinc are not preferable, because if the capacitors incorporated in the printed circuit board have a film including these metals formed on their electrodes, a migration is easily generated at a connection with the via holes.

The surfaces of the chip capacitors may be roughened. The rough surface contributes to an increased adhesion between the chip capacitors made of ceramic, and a connection layer and a resin insulating layer made of resin, thereby avoiding the resin insulating layer from peeling from the interface with the chip capacitors even when a heat cycle test is conducted.

In the invention recited in claim 6, the chip capacitors are accommodated in the printed circuit board in the state where at least a part of the electrodes of each capacitor is uncoated with a coating layer and

exposed to the outside. An electric connection for the electrode exposed from the coating layer is established. The metal exposed from the coating layer includes copper as a main component, because the connection resistance
5 can be lowered.

In the invention recited in claim 7, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used. With this arrangement, a large space can be used for external electrodes even
10 if a conduction is established through the via holes, and therefore, the broadened range of alignment is allowed. As a result, a problem of disconnection is eliminated.

In the invention recited in claim 8, a chip
15 capacitor in which electrodes are formed in matrix is used. It becomes easy to accommodate a large chip capacitor in a core substrate. Therefore, it becomes possible to increase an electrostatic capacity, and a problem concerning electricity can be solved. In
20 addition, warpage is hard to generate in the printed circuit board even if the printed circuit board undergoes various thermal histories.

A plurality of chip capacitors from each of which a plurality of pieces are to be obtained may be coupled
25 into one piece unit and used. In this manner, an electrostatic capacity can be properly adjusted and the IC chip can be properly operated.

In the invention recited in claim 9, a capacitor
30 is mounted on the surface of the printed circuit board on top of the capacitors accommodated in the substrate. Since the capacitors are accommodated within the printed circuit board, the distance between the IC chip and each capacitor is shortened. In addition, the loop

inductance can be lowered, and electric power can be instantaneously provided. On the other hand, since a capacitor is provided on the surface of the printed circuit board as well, a capacitor having a large capacity can be mounted. In this manner, large electric power can be easily supplied to the IC chip.

A method for manufacturing a printed circuit board according to claim 10 is characterized by comprising at least the following steps (a) to (c):

- (a) forming a cavity in a core substrate;
- (b) mounting a plurality of capacitors in the cavity; and
- (c) charging a resin between the capacitors.

In the invention recited in claim 10, a large cavity is formed in a core substrate. With this arrangement, a plurality of capacitors can be reliably provided in the core substrate. In addition, since a plurality of capacitors are mounted in the cavity, the plurality of capacitors are aligned to the same heights with each other. As a result, the surface of the core substrate becomes flat and smooth. In addition, the cavity is formed in such a manner as to have a large area, the capacitors can be located at accurate positions. The interlayer resin insulating layer and the conductor circuit can be properly formed on the core substrate without impairing the flatness and smoothness of the core substrate. Therefore, the rate of generating defective printed circuit boards can be lowered. In addition, a resin is charged between the capacitors, the capacitors can be fixed in the cavity after the positions of capacitors are determined within the cavity.

In the invention recited in claim 11, a pressure is applied to the upper surfaces of the plurality of

capacitors in the cavity, or tapped to align the chip capacitors into the same heights with each other. By this process, even if chip capacitors having largely different sizes from each other are provided in the cavity, they are aligned into the completely same heights with each other. As a result, the core substrate can have a flat and smooth surface. The interlayer resin insulating layer and the conductor circuit as upper layers can be properly formed on the core substrate without impairing the flatness and smoothness of the core substrate, and therefore, the rate of generating defective printed circuit boards can be lowered.

In the invention recited in claim 12, a through hole is formed between the capacitors in the resin layer. A signal line does not pass through the chip capacitors. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. The through holes enable the establishment of the electric connection between the top and bottom surfaces of the printed circuit board. It is possible to provide wires under the capacitors through the buildup layer, and therefore, pins and BGAs of the capacitors can be provided.

A method for manufacturing a printed circuit board according to claim 13 is characterized by comprising at least the following steps (a) to (c):

(a) forming penetrating openings in a resin material having a core material impregnated with a resin;

(b) attaching a resin material to the resin material formed with the penetrating openings to form a core substrate having a cavity;

(c) mounting a plurality of capacitors in the cavity of the core substrate; and
(d) charging a resin between the capacitors.

In the invention recited in claim 13, a large
5 cavity is formed in a core substrate. With this arrangement, a plurality of capacitors can be reliably provided in the core substrate. In addition, since a plurality of capacitors are mounted in the cavity, the plurality of capacitors are aligned to the same heights
10 with each other. As a result, the surface of the core substrate becomes flat and smooth. In addition, the cavity is formed in such a manner as to have a large area, the capacitors can be located at accurate positions. The interlayer resin insulating layer and the conductor
15 circuit can be properly formed on the core substrate without impairing the flatness and smoothness of the core substrate. Therefore, the rate of generating defective printed circuit boards can be lowered. In addition, a resin is charged between the capacitors, the capacitors
20 can be fixed in the cavity after the positions of capacitors are determined within the cavity.

In the invention recited in claim 14, a pressure is applied to the upper surfaces of the plurality of capacitors in the cavity, or tapped to align the chip
25 capacitors into the same heights with each other. By this process, even if chip capacitors having largely different sizes from each other are provided in the cavity, they are aligned into the completely same heights with each other. As a result, the core substrate can have a
30 flat and smooth surface. The interlayer resin insulating layer and the conductor circuit can be properly formed on the core substrate without impairing the flatness and smoothness of the core substrate, and

therefore, the rate of generating defective printed circuit boards can be lowered.

In the invention recited in claim 15, since through holes are formed between the capacitors in the resin layer, a signal line does not pass through the chip capacitors. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. The through holes enables the establishment of the electric connection between the top and bottom surfaces of the printed circuit board. It is possible to provide wires under the capacitors through the buildup layer, and therefore, pins and BGAs of the capacitors can be provided.

In order to solve the above problem, a printed circuit board according to claim 16 is characterized by comprising a core substrate, and a resin insulating layer and a conductor circuit laminated on the core substrate,

wherein the core substrate incorporates a connection layer formed by an insulating resin layer including at least one or more layer, and an accommodation layer accommodating a capacitor in its spot-faced section.

- It means the circuit formed by buildup method where an interlayer resin insulating layer is formed on the core substrate, and via holes or through holes are formed in the interlayer resin insulating layer to form a conductor circuit as a conductive layer. As the buildup layer, a semi-additive method or a fully-additive method may be employed.

In the invention recited in claim 16, capacitors are mounted within the printed circuit board. In this

manner, the distance between the IC chip and each capacitor is shortened, and the loop inductance can be lowered. The core substrate incorporates one or more connection layers and an accommodation layer for accommodating the capacitors. Since the capacitors are accommodated within the accommodation layer having large thickness, the thickness of the core substrate does not become large. The thickness of the printed circuit board does not become large even if the interlayer resin insulating layer and the conductor circuit are laminated on the core substrate.

It is desirable to fill the cavity with a resin. As a result, the behavior of the capacitors incorporated in the core substrate becomes small. In addition, even if the stress is generated caused by the capacitors, the stress can be alleviated by the resin. The resin also has an effect of adhering the capacitors to the core substrate, and lowering a migration between the capacitors and the core substrate.

In the invention recited in claim 17, an accommodation layer is constituted by a resin substrate having a core material impregnated with a resin. As a result, sufficiently high strength can be given to the core substrate.

In the invention recited in claim 18, the connection layer and the capacitors accommodated in the accommodation layer are connected to each other through a conductive adhesive. In this manner, the electrical connection with the capacitors and the adhesion between the capacitors and the connection layer can be assured. The conductive adhesive may be a material having both conductivity and adhesiveness such as a solder (Sn/Pb, Sn/Sb, Sn/Ag, Sn/Ag/Cu), conductive pastes, and resins

impregnated with metal particles.

The space created between the conductive adhesive and the capacitor is preferably filled with a resin, because, in this manner, the behavior derived from the capacitors can be alleviated and the migration of the conductive adhesive can be prevented.

In the invention recited in claim 19, a circuit which is connected to the conductive adhesive is provided between the connection layer and the accommodation layer. In this manner, a connection with the capacitors can be reliably established through the circuit. By providing a circuit constituted by a metal layer between the connection layer and the accommodation layer, the warpage of the core substrate can be prevented.

In the invention recited in claim 20, an external substrate (i.e. daughter board, mother board) to be connected to the back surface of the printed circuit board is connected to the terminals of the capacitor through the via holes formed in the connection layer and the through holes formed in the core substrate. That is, although the accommodation layer having a core material is hard to process, though holes are formed in the accommodation layer so that the terminals of the capacitors are not directly connected to the outside surface. As a result, the reliability of the connection can be increased.

In the invention recited in claim 21, a wiring for connecting an IC chip and an external substrate is provided between capacitors, and a signal line does not pass through the chip capacitors. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by

passing through the high dielectric body. By mounting a capacitor for power supply, large electric power can be easily supplied to the IC chip. Furthermore, noise generated when a signal is transmitted in the printed circuit board can be reduced.

In addition, by providing a wiring for connection, it becomes possible to provide a wiring below the capacitors. In this manner, a wiring has an increased degree of freedom, thereby attaining high density and small size.

In the invention recited in claim 22, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used. With this arrangement, a large space can be used for external electrodes even if a conduction is established through the via holes, and therefore, the broadened range of alignment is allowed. As a result, a problem of disconnection is eliminated.

In the invention recited in claim 23, a chip capacitor in which electrodes are formed in matrix is used. It becomes easy to accommodate a large chip capacitor in a core substrate. Therefore, it becomes possible to increase an electrostatic capacity, and a problem concerning electricity can be solved. In addition, warpage is hard to generate in the printed circuit board even if the printed circuit board undergoes various thermal histories.

A plurality of chip capacitors from each of which a plurality of pieces are to be obtained may be coupled to each other into one piece unit and used. In this manner, an electrostatic capacity can be properly adjusted and the IC chip can be properly operated.

In the invention recited in claim 24, a capacitor

is mounted on the surface of the printed circuit board on top of the capacitors accommodated in the substrate. Since the capacitors are accommodated within the printed circuit board, the distance between the IC chip and each capacitor is shortened. In addition, the loop inductance can be lowered, and electric power can be instantaneously provided. On the other hand, since a capacitor is provided on the surface of the printed circuit board as well, a capacitor having a large capacity can be mounted. In this manner, large electric power can be easily supplied to the IC chip.

In the invention recited in claim 25, the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably exhibits a desired operation.

In the invention recited in claim 26, the chip capacitor mounted on the surface of the printed circuit board has an inductance same or smaller than the inductance of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably exhibits a desired operation.

The surface of the chip capacitor may be subjected to roughening treatment. The rough surface contributes to an increased adhesion between the chip capacitor made of ceramic and a connection layer and a resin insulating layer made of resin, thereby avoiding the connection layer and the interlayer resin insulating layer from peeling from the interface with the chip capacitors even

when a heat cycle test is conducted.

In the invention recited in claim 27, copper is provided around the respective chip capacitors. In this manner, no migration is generated in the capacitors incorporated in the printed circuit board. In addition, the capacitors never peel from the resin charged between the capacitors, and no cracks are created. The accommodation characteristic is enhanced, and as a result, there is no deterioration in electric characteristics.

In the invention recited in claim 28, a resin is charged between the spot-faced section of the core substrate and the capacitor. The thermal expansion coefficient of the resin is set to the value lower than the thermal expansion coefficient of the core substrate, that is, is set to the value close to that of the chip capacitor made of ceramics. In this manner, even if internal stress is generated between the core substrate and the resin insulating layer, and the chip capacitor caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur. As a result, high reliability can be attained. In addition, the generation of migration can be prevented.

A method for manufacturing a printed circuit board according to claim 29 is characterized by comprising at least the following steps (a) to (c):

(a) forming a circuit pattern on a resin plate on its one side or both sides, and connecting a capacitor to the circuit pattern through an adhesive material;

(b) attaching a resin substrate formed with a cavity for accommodating the capacitor to the resin plate to form a core substrate; and

(c) forming openings extending to electrodes of

the capacitor in the resin plate to form via holes.

In the method for manufacturing a printed circuit board of the invention recited in claim 29, it becomes possible to accommodate chip capacitors in a core substrate. As a result, a printed circuit board having
5 a lowered loop inductance can be provided.

In the method for manufacturing a printed circuit board of the invention recited in claim 30, a resin substrate accommodating capacitors and a resin plate are
10 attached to each other by applying a pressure from both sides to form a core substrate. Thus-formed core substrate has a flat surface. As a result, an interlayer resin insulating layer and a conductor circuit having high reliability can be laminated on the core substrate.

In the method for manufacturing a printed circuit
15 board of the invention recited in claim 31, a through hole for an IC chip and an external substrate is provided between capacitors. A signal line does not pass through the chip capacitors 20 made of ceramics. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. By mounting
20 a capacitor for power supply, it becomes possible to easily provide large electric power to the IC chip.
25

In order to solve the above-described problems, in the invention recited in claim 32, a printed circuit board incorporates a core substrate, and a resin insulating layer and a conductor circuit laminated to
30 a core substrate. The core substrate incorporates a connection layer formed by an insulating resin layer including at least one or more layer, and an accommodation layer formed by a resin layer accommodating capacitors

and including two or more layers.

It means the circuit formed by buildup method where an interlayer resin insulating layer is formed on the core substrate, and via holes or through holes are formed
5 in the interlayer resin insulating layer to form a conductor circuit as a conductive layer. As the buildup layer, a semi-additive method or a fully-additive method may be employed.

In the invention recited in claim 32, capacitors
10 are mounted within the printed circuit board. In this manner, the distance between the IC chip and each capacitor is shortened, and the loop inductance can be lowered. The core substrate incorporates one or more connection layers and an accommodation layer for
15 accommodating the capacitors. Since the capacitors are accommodated within the accommodation layer having large thickness, the thickness of the core substrate does not become thick. The thickness of the printed circuit board does not become thick even if the interlayer resin
20 insulating layer and the conductor circuit are laminated on the core substrate.

It is desirable to fill the cavity with a resin. As a result, the behavior of the capacitors incorporated in the core substrate becomes small. In addition, even
25 if the stress is generated caused by the capacitors, the stress can be alleviated by the resin. The resin also has an effect of adhering the capacitors to the core substrate, and lowering a migration between the capacitors and the core substrate.

30 A printed circuit board according to claim 33 is characterized by comprising a resin insulating layer and a conductor circuit laminated to the core substrate, wherein the core substrate incorporates a

connection layer formed by an insulating resin layer including at least one or more layer, and an accommodation layer formed by a resin layer accommodating a capacitor and including two or more layers, and vias for establishing a connection with the capacitor are formed on both sides of the core substrate.

In the invention recited in claim 33, capacitors are mounted within the printed circuit board. In this manner, the distance between the IC chip and each capacitor is shortened, and the loop inductance can be lowered. The core substrate is constituted by at least one or more connection layer and an accommodation layer for accommodating the capacitors. Since the capacitors are accommodated within the accommodation layer having large thickness, the thickness of the core substrate does not become large. The thickness of the printed circuit board does not become large even if the interlayer resin insulating layer and the conductor circuit are laminated on the core substrate. Furthermore, since vias to be connected to the capacitors are formed on both sides, the wire length from the capacitors to the IC chip and the external substrate is shortened.

In the invention recited in claim 36, a wiring for connecting an IC chip and an external substrate is provided between capacitors, and a signal line does not pass through the chip capacitors. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. By mounting a capacitor for power supply, large electric power can be easily supplied to the IC chip. Furthermore, by providing a capacitor for ground, noise generated when

a signal is transmitted in the printed circuit board can be reduced.

In addition, by providing a wiring for connection, it becomes possible to provide a wiring below the capacitors. In this manner, a wiring has an increased degree of freedom, thereby attaining high density and small size.

In the invention recited in claim 37, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used. With this arrangement, a large space can be used for external electrodes even if a conduction is established through the via holes, and therefore, the broadened range of alignment is allowed. As a result, a problem of disconnection is eliminated.

In the invention recited in claim 38, a chip capacitor in which electrodes are formed in matrix is used. It becomes easy to accommodate a large chip capacitor in a core substrate. Therefore, it becomes possible to increase an electrostatic capacity, and a problem concerning electricity can be solved. In addition, warpage is hard to generate in the printed circuit board even if the printed circuit board undergoes various thermal histories.

A plurality of chip capacitors from each of which a plurality of pieces are to be obtained may be coupled to each other into one piece unit and used. In this manner, an electrostatic capacity can be properly adjusted and the IC chip can be properly operated.

In the invention recited in claim 39, a capacitor is mounted on the surface of the printed circuit board on top of the capacitors accommodated in the substrate. Since the capacitors are accommodated within the printed

circuit board, the distance between the IC chip and each capacitor is shortened. In addition, the loop inductance can be lowered, and electric power can be instantaneously provided. On the other hand, since a
5 capacitor is provided on the surface of the printed circuit board as well, a capacitor having a large capacity can be mounted. In this manner, large electric power can be easily supplied to the IC chip.

In the invention recited in claim 40, the chip
10 capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high
15 frequency domain, and the IC chip reliably exhibits a desired operation.

In the invention recited in claim 41, the chip
capacitor mounted on the surface of the printed circuit board has an inductance same or larger than the inductance
20 of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably exhibits a desired operation.

In the invention recited in claims 42 and 43, an
25 electric connection for electrodes formed with a metal film of the capacitors is established by via holes formed by plating. The electrodes of the chip capacitor are made by metallizing, and have pits and projections on their surfaces. However, the surfaces become smooth by
30 formation of the metal film, and the via holes are then formed on the smooth surfaces. In this manner, when penetrating openings are formed in the resin coating the electrodes, no resin remains, and a reliability of the

connection between the via holes and the electrodes can be increased. Furthermore, since the via holes are made by plating into the electrodes formed with the copper plated film, the electrodes are firmly connected to the via holes. No disconnection occurs between the electrodes and via holes even when a heat cycle test is conducted.

The metal film formed on the electrodes of the capacitors preferably includes any one of metals selected from the group consisting of copper, nickel, and noble metals. Tins and zinc are not preferable, because if the capacitors incorporated in the printed circuit board have a film including these metals formed on their electrodes, a migration is easily generated at a connection with the via holes.

The surfaces of the chip capacitors may be roughened. The rough surface contributes to an increased adhesion between the chip capacitor made of ceramic, and a connection layer and a resin insulating layer made of resin, thereby avoiding the resin insulating layer from peeling from the interface with the chip capacitor even when a heat cycle test is conducted.

In the invention recited in claim 44, the chip capacitors are accommodated in the printed circuit board in the state where at least a part of the electrodes of each capacitor is uncoated with a coating layer and exposed to the outside. An electric connection for the electrode exposed from the coating layer is established. The metal exposed from the coating layer preferably includes copper as a main component, because the connection resistance can be lowered.

In the invention recited in claim 45, the thermal

expansion coefficient of the insulating adhesive is set to the value lower than the thermal expansion coefficient of the accommodating layer, that is, is set to the value close to that of the chip capacitor made of ceramics.

5 In this manner, even if internal stress is generated between the core substrate and the resin insulating layer, and the chip capacitor caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur when a heat cycle test is
10 conducted. As a result, high reliability can be attained.

A method for manufacturing a printed circuit board according to claim 46 is characterized by comprising at least the following steps (a) to (e):

(a) forming penetrating openings for
15 accommodating a capacitor in a first resin material having a core material impregnated with a resin;

(b) attaching a second resin material to the first resin material formed with the penetrating openings to form an accommodation layer having a section for
20 accommodating a capacitor;

(c) accommodating the capacitor in the accommodation layer;

(d) attaching a third insulating resin layer to the accommodation layer formed in the step (c) to form
25 a core substrate; and

(e) forming openings extending to electrodes of the capacitor in the third insulating resin layer to form via holes.

A method for manufacturing a printed circuit board
30 according to claim 47 is characterized by comprising at least the following steps (a) to (e):

(a) forming penetrating openings for accommodating a capacitor in a first resin material

having a core material impregnated with a resin;

(b) providing a capacitor to the second resin material at a position corresponding to a section for accommodating a capacitor in the resin material;

5 (c) attaching the first resin material subjected to the step (a) and the second resin material subjected to the step (b) to each other to form an accommodation layer accommodating the capacitor;

10 (d) attaching a third insulating resin layer to the accommodation layer to form a core substrate; and

(e) forming openings in the third insulating resin layer extending to electrodes of the capacitor to form via holes.

15 A method for manufacturing a printed circuit board according to claim 48 is characterized by comprising at least the following steps (a) to (f):

(a) forming penetrating openings for accommodating a capacitor in a first resin material having a core material impregnated with a resin;

20 (b) providing a capacitor to the second resin material at a position corresponding to a section for accommodating a capacitor in the resin material;

25 (c) attaching the first resin material subjected to the step (a) and the second resin material subjected to the step (b) to each other to form an accommodation layer accommodating the capacitor;

(d) attaching a third insulating resin layer to the accommodation layer to form a core substrate;

30 (e) forming openings in the third insulating resin layer extending to electrodes of the capacitor to form via holes; and

(f) forming a conductive film in the penetrating openings of the first resin material and the openings

of the third resin material to form via holes.

In the method for manufacturing a printed circuit board of the invention recited in claims 46 and 47, it becomes possible to accommodate chip capacitors in a core substrate. As a result, a printed circuit board having a lowered loop inductance can be provided.

In the method for manufacturing a printed circuit board of the invention recited in claim 48, it becomes possible to accommodate chip capacitors in a core substrate. As a result, a printed circuit board having a lowered loop inductance can be provided. Since via holes are formed on both surfaces of the core substrate, the wire length from the capacitors to the IC chip and the external substrate is shortened.

In the method for manufacturing a printed circuit board of the invention recited in claim 49, a resin substrate accommodating capacitors and a resin plate are attached to each other by applying a pressure from both sides to form a core substrate. Thus-formed core substrate has a flat surface. As a result, an interlayer resin insulating layer and a conductor circuit having high reliability can be laminated on the core substrate.

A printed circuit board according to claim 50 is characterized by comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

wherein the core substrate incorporates an accommodating layer having penetrating openings in each of which a capacitor is accommodated, and connection layers each made of an insulating resin layer and provided on the front surface and the back surface of the accommodation layer.

It means the circuit formed by buildup method where

an interlayer resin insulating layer is formed on the core substrate, and via holes or through holes are formed in the interlayer resin insulating layer to form a conductor circuit as a conductive layer. As the buildup layer, a semi-additive method or a fully-additive method may be employed.

In the invention recited in claim 50, capacitors are mounted within the printed circuit board. In this manner, the distance between the IC chip and each capacitor is shortened, and the loop inductance can be lowered. The core substrate incorporates at least one or more connection layers and an accommodation layer for accommodating the capacitors. Since the capacitors are accommodated within the accommodation layer having large thickness, the thickness of the core substrate does not become large. The thickness of the printed circuit board does not become large even if the interlayer resin insulating layer and the conductor circuit are laminated on the core substrate.

Since via holes are formed on both surfaces of the core substrate, the power supply located on the substrate connected to the outside and the capacitors accommodated in the substrate can be connected to each other in a shortest distance. With this arrangement, a voltage can be instantaneously supplied from the power supply to the IC chip, and the voltage for driving the IC can be promptly stabilized.

The cavity is preferably filled with a resin. The resin eliminates a space between the capacitors and the core substrate. As a result, the behavior of the capacitors incorporated in the core substrate becomes small. In addition, even if the stress is generated caused by the capacitors, the stress can be alleviated

by the resin. The resin also has an effect of adhering the capacitors to the core substrate, and lowering a migration between the capacitors and the core substrate.

In the invention recited in claim 51, an accommodation layer is constituted by a resin substrate having a core material impregnated with a resin. As a result, sufficiently high strength can be given to the core substrate.

In the invention recited in claim 52, the capacitors are fixed in the penetrating openings of the accommodation layer through an insulating adhesive. In this manner, the capacitors can be fixed to proper positions.

In the invention recited in claim 53, the IC chip mounted on the front surface of the printed circuit board, the external substrate mounted on the back surface of the printed circuit board (i.e. daughter board, mother board) are connected to the terminals of the capacitors through the via holes formed in the connection layer. That is, the terminals of the capacitors, the IC chip, and the external substrate are directly connected to each other. As a result, the length of electric wire can be shortened.

In the invention recited in claim 54, a wiring for connecting an IC chip and an external substrate is provided between capacitors, and a signal line does not pass through the chip capacitors. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. By mounting a capacitor for power supply, large electric power can be easily supplied to the IC chip. Furthermore, by

providing a capacitor for ground, noise generated when a signal is transmitted in the printed circuit board can be reduced. In addition, by providing a wiring for connection, it becomes possible to provide a wiring below
5 the capacitors. In this manner, a wiring has an increased degree of freedom, thereby attaining high density and small size.

In the invention recited in claim 55, a capacitor is mounted on the surface of the printed circuit board
10 on top of the capacitors accommodated in the substrate. Since the capacitors are accommodated within the printed circuit board, the distance between the IC chip and each capacitor is shortened. In addition, the loop inductance can be lowered, and electric power can be
15 instantaneously provided. On the other hand, since a capacitor is provided on the surface of the printed circuit board as well, a capacitor having a large capacity can be mounted. In this manner, large electric power can be easily supplied to the IC chip.

In the invention recited in claim 56, the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board. In this
20 manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably exhibits a desired operation.

In the invention recited in claim 57, the chip capacitor mounted on the surface of the printed circuit board has an inductance same or larger than the inductance
30 of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably

exhibits a desired operation

In the invention recited in claim 58, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used. With this arrangement, a large space can be used for external electrodes even if a conduction is established through the via holes, and therefore, the broadened range of alignment is allowed. As a result, a problem of disconnection is eliminated.

In the invention recited in claim 59, a chip capacitor in which electrodes are formed in matrix is used. It becomes easy to accommodate a large chip capacitor in a core substrate. Therefore, it becomes possible to increase an electrostatic capacity, and a problem concerning electricity can be solved. In addition, warpage is hard to generate in the printed circuit board even if the printed circuit board undergoes various thermal history.

A plurality of chip capacitors which are coupled to each other into one piece unit and from each of which a plurality of pieces are to be obtained may be used. In this manner, an electrostatic capacity can be properly adjusted and the IC chip can be properly operated.

In the invention recited in claims 60 and 61, an electric connection for electrodes formed with a metal film of the capacitors is established by via holes formed by plating. The electrodes of the chip capacitor are made by metallizing, and have pits and projections on their surfaces. However, the surfaces become smooth by formation of the metal film, and the via holes are then formed on the smooth surfaces. In this manner, when penetrating openings are formed in the resin coating the electrodes, no resin remains, and a reliability of the

connection between the via holes and the electrodes can be increased. Furthermore, since the via holes are made by plating into the electrodes formed with the copper plated film, the electrodes are firmly connected to the via holes. No disconnection occurs between the electrodes and via holes even when a heat cycle test is conducted.

The metal film formed on the electrodes of the capacitors preferably includes any one of metals selected from the group consisting of copper, nickel, and noble metals. Tins and zinc are not preferable, because if the capacitors incorporated in the printed circuit board has a film including these metals formed on their electrodes, a migration is easily generated at a connection with the via holes.

The surfaces of the chip capacitors may be roughened. The rough surface contributes to an increased adhesion between the chip capacitor made of ceramic and a resin insulating layer made of resin, thereby avoiding the resin insulating layer from peeling from the interface with the chip capacitor even when a heat cycle test is conducted.

In the invention recited in claim 62, the chip capacitors are accommodated in the printed circuit board in the state where at least a part of the electrodes of each capacitor is uncoated with a coating layer and exposed to the outside. An electric connection for the electrode exposed from the coating layer is established. The metal exposed from the coating layer preferably includes copper as a main component, because the connection resistance can be lowered.

In the invention recited in claim 63, the thermal expansion coefficient of the resin is set to the value

lower than the thermal expansion coefficient of the core substrate, that is, is set to the value close to that of the chip capacitor made of ceramics. In this manner, even if internal stress is generated between the core substrate and the resin insulating layer, and the chip capacitor caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur when a heat cycle test is conducted. As a result, high reliability can be attained. In addition, the generation of migration can be prevented.

A method for manufacturing a printed circuit board according to claim 64 is characterized by comprising at least the following steps (a) to (d):

(a) forming penetrating openings for accommodating a capacitor in a first resin material having a core material impregnated with a resin;

(b) accommodating a capacitor in each of the penetrating openings of the first resin material;

(c) attaching a second resin material to the first resin material to form a core substrate; and

(d) forming openings extending to electrodes of the capacitor in the second resin material of the core substrate to form via holes.

In the method for manufacturing a printed circuit board of the invention recited in claim 64, it becomes possible to accommodate chip capacitors in a core substrate. As a result, a printed circuit board having a lowered loop inductance can be provided.

In the invention recited in claim 65, a wiring for connecting an IC chip and an external substrate is provided between capacitors, and a signal line does not pass through the chip capacitors. This structure

eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. By mounting
5 a capacitor for power supply, large electric power can be easily supplied to the IC chip.

In the method for manufacturing a printed circuit board of the invention recited in claim 66, a resin substrate accommodating capacitors and a resin plate are
10 attached to each other by applying a pressure from both sides to form a core substrate. Thus-formed core substrate has a flat surface. As a result, an interlayer resin insulating layer and a conductor circuit having high reliability can be laminated on the core substrate.

In order to solve the above-described problems,
15 in the invention recited in claim 67, a printed circuit board incorporates a core substrate, and a resin insulating layer and a conductor circuit laminated to a core substrate. The capacitors are accommodated in
20 the core substrate.

It means the circuit formed by buildup method where an interlayer resin insulating layer is formed on the core substrate, and via holes or through holes are formed in the interlayer resin insulating layer to form a
25 conductor circuit as a conductive layer. As the buildup layer, a semi-additive method or a fully-additive method may be employed.

In the invention recited in claim 67, capacitors are mounted within the printed circuit board. In this
30 manner, the distance between the IC chip and each capacitor is shortened, and the loop inductance can be lowered. Since the capacitors are accommodated within the accommodation layer having large thickness, the

thickness of the core substrate does not become thick.
The thickness of the printed circuit board does not become
thick even if the interlayer resin insulating layer and
the conductor circuit are laminated on the core
5 substrate.

It is desirable to fill the cavity with a resin.
As a result, the behavior of the capacitors incorporated
in the core substrate becomes small. In addition, even
if the stress is generated caused by the capacitors, the
10 stress can be alleviated by the resin. The resin also
has an effect of adhering the capacitors to the core
substrate, and lowering a migration between the
capacitors and the core substrate.

A printed circuit board according to claim 68 is
15 characterized by comprising a core substrate, and a resin
insulating layer and a conductor circuit laminated to
the core substrate,
wherein the chip capacitor is accommodated in the printed
circuit board in the state where at least a part of
20 electrodes of each capacitor is uncoated with a coating
layer and exposed to the outside, and an electric
connection for the electrode exposed from the coating
layer is established by plating.

In the invention recited in claims 68 and 69, the
25 chip capacitors are accommodated in the printed circuit
board in the state where at least a part of the electrodes
of each capacitor is uncoated with a coating layer and
exposed to the outside. An electric connection for the
electrode exposed from the coating layer is established.
30 The metal exposed from the coating layer includes
preferably copper as a main component. This is because
the connection to the exposed metal provided with plating
is increased, and as a result, the difference in electric

characteristics is cancelled and the connection resistance can be lowered.

A printed circuit board according to claim 70 is characterized by comprising a core substrate, and a resin
5 insulating layer and a conductor circuit laminated to the core substrate,

wherein the chip capacitor is accommodated in the state where a metal film is formed on electrodes of the capacitor, and an electric connection for the electrodes formed with
10 the metal film is established by plating.

In the invention recited in claims 70 and 71, an electric connection for electrodes formed with a metal film of the capacitors is established by via holes formed by plating. The electrodes of the chip capacitor are
15 made by metallizing, and have pits and projections on their surfaces. However, the surfaces become smooth by formation of the metal film, and the via holes are then formed on the smooth surfaces. In this manner, when penetrating openings are formed in the resin coating the
20 electrodes, no resin remains, and a reliability of the connection between the via holes and the electrodes can be increased. Furthermore, since the via holes are made by plating into the electrodes formed with the copper plated film, the electrodes are firmly connected to the
25 via holes. No disconnection occurs between the electrodes and via holes even when a heat cycle test is conducted.

The metal film formed on the electrodes of the capacitors preferably includes any one of metals
30 selected from the group consisting of copper, nickel, and noble metals. Tins and zinc are not preferable, because if the capacitors incorporated in the printed circuit board has a film including these metals formed

on their electrodes, a migration is easily generated at a connection with the via holes. Since tins and zinc are not used in the present invention, the generation of migration can be prevented.

5 In the invention recited in claim 72, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used. With this arrangement, a large space can be used for external electrodes even if a conduction is established through the via holes, 10 and therefore, the broadened range of alignment is allowed. As a result, a problem of disconnection is eliminated.

In the invention recited in claim 73, a chip capacitor in which electrodes are formed in matrix is 15 used. It becomes easy to accommodate a large chip capacitor in a core substrate. In addition, warpage is hard to generate in the printed circuit board even if the printed circuit board undergoes various thermal histories.

20 In the invention recited in claim 74, a plurality of chip capacitors from each of which a plurality of pieces are to be obtained may be coupled to each other into one piece unit and used. In this manner, an electrostatic capacity can be properly adjusted and the IC chip can 25 be properly operated.

A printed circuit board according to claim 75 is characterized by comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

30 wherein a capacitor is accommodated in the core substrate, and a capacitor is mounted on the surface of the printed circuit board.

In the invention recited in claim 75, a capacitor

is mounted on the surface of the printed circuit board on top of the capacitors accommodated in the substrate. Since the capacitors are accommodated within the printed circuit board, the distance between the IC chip and each capacitor is shortened. In addition, the loop inductance can be lowered, and electric power can be instantaneously provided. On the other hand, since a capacitor is provided on the surface of the printed circuit board as well, a capacitor having a large capacity can be mounted. In this manner, large electric power can be easily supplied to the IC chip.

In the invention recited in claim 76, the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably exhibits a desired operation.

In the invention recited in claim 77, the chip capacitor mounted on the surface of the printed circuit board has an inductance same or larger than the inductance of the chip capacitor incorporated in the printed circuit board. In this manner, there is no shortage of power supply at a high frequency domain, and the IC chip reliably exhibits a desired operation.

The surface of the chip capacitor may be subjected to roughening treatment. The rough surface contributes to an increased adhesion between the chip capacitor made of ceramic, and a connection layer and a resin insulating layer made of resin, thereby avoiding the connection layer and the interlayer resin insulating layer from peeling from the interface with the chip capacitor even

when a heat cycle test is conducted.

In the invention recited in claim 78, a copper plated film is coated on the surface of a metallized electrodes of a chip capacitor.

5 In the invention recited in claim 78, a metal film is formed on the electrodes of the chip capacitors. As a result, the chip capacitor have a flat surface. When the chip capacitors are accommodated in the printed circuit board, and penetrating openings are formed in
10 the resin which covers the electrodes, no resin is left. In this manner, the connection between the via holes and the electrodes has increased reliability.

Brief Description of Drawings

15 Fig. 1 is a diagram showing a process for manufacturing a printed circuit board according to a first embodiment of the present invention.

Fig. 2 is a diagram showing a process for manufacturing a printed circuit board according to a
20 first embodiment.

Fig. 3 is a diagram showing a process for manufacturing a printed circuit board according to a first embodiment.

Fig. 4 is a diagram showing a process for
25 manufacturing a printed circuit board according to a first embodiment.

Fig. 5 is a diagram showing a process for manufacturing a printed circuit board according to a first embodiment.

30 Fig. 6 is a diagram showing a process for manufacturing a printed circuit board according to a first embodiment.

Fig. 7 is a diagram showing a cross section of

the printed circuit board according to a first embodiment.

Fig. 8 is a diagram showing a cross section of the state where an IC chip is mounted on the printed circuit board according to the first embodiment.

Fig. 9 is a diagram showing a process for manufacturing a printed circuit board according to a first modification of the first embodiment.

Fig. 10 is a diagram showing a process for manufacturing a printed circuit board according to a first modification of the first embodiment.

Fig. 11 is a diagram showing a process for manufacturing a printed circuit board according to a first modification of the first embodiment.

Fig. 12 is a diagram showing a process for manufacturing a printed circuit board according to a first modification of the first embodiment.

Fig. 13 is a diagram showing a process for manufacturing a printed circuit board according to a first modification of the first embodiment.

Fig. 14 is a diagram showing a process for manufacturing a printed circuit board according to a first modification of the first embodiment.

Fig. 15 is a diagram showing a cross section of the state where an IC chip is mounted on the printed circuit board according to the first modification of the first embodiment.

Fig. 16 is a diagram showing a process for manufacturing a printed circuit board according to a second modification of the first embodiment.

Fig. 17 is a diagram showing a cross section of the chip capacitor according to the first embodiment.

Fig. 18 is a plan view showing a chip capacitor

according to a third modification of the first embodiment.

Fig. 19 is a plan view showing a chip capacitor according to a third modification of the first
5 embodiment.

Fig. 20 is a plan view showing a chip capacitor according to a third modification of the first embodiment.

Fig. 21 is a diagram showing a cross section of
10 the printed circuit board according to a fourth modification of the first embodiment.

Fig. 22 is a graph showing the changes in the voltage supplied to the IC chip and the time.

Fig. 23 is a diagram showing a process for
15 manufacturing a printed circuit board according to a second embodiment of the present invention.

Fig. 24 is a diagram showing a process for manufacturing a printed circuit board according to a second embodiment.

Fig. 25 is a diagram showing a process for
20 manufacturing a printed circuit board according to a second embodiment.

Fig. 26 is a diagram showing a process for manufacturing a printed circuit board according to a
25 second embodiment.

Fig. 27 is a diagram showing a process for manufacturing a printed circuit board according to a second embodiment.

Fig. 28 is a diagram showing a process for
30 manufacturing a printed circuit board according to a second embodiment.

Fig. 29 is a diagram showing a cross section of the printed circuit board according to a second

embodiment.

Fig. 30 is a diagram showing a cross section of the printed circuit board according to a second embodiment.

5 Fig. 31 is a diagram showing a cross section of the printed circuit board according to a first modification of the second embodiment.

Fig. 32 is a diagram showing a cross section of the printed circuit board according to a second
10 modification of the second embodiment.

Fig. 33 is a diagram showing a cross section of the printed circuit board according to a third modification of the second embodiment.

Fig. 34 is a diagram showing a process for
15 manufacturing a printed circuit board according to a third embodiment of the present invention.

Fig. 35 is a diagram showing a process for manufacturing a printed circuit board according to a third embodiment.

20 Fig. 36 is a diagram showing a process for manufacturing a printed circuit board according to a third embodiment.

Fig. 37 is a diagram showing a cross section of the printed circuit board according to a third
25 embodiment.

Fig. 38 is a diagram showing a cross section of the printed circuit board according to a third embodiment.

Fig. 39 is a diagram showing a cross section of
30 the printed circuit board according to a first modification of the third embodiment.

Fig. 40 is a diagram showing a process for manufacturing a printed circuit board according to a

second modification of the third embodiment.

Fig. 41 is a diagram showing a process for manufacturing a printed circuit board according to a second modification of the third embodiment.

5 Fig. 42 is a diagram showing a cross section of the printed circuit board according to a second modification of the third embodiment.

Fig. 43 is a diagram showing a process for manufacturing a printed circuit board according to third
10 modification of the third embodiment.

Fig. 44 is a diagram showing a cross section of the printed circuit board according to a third modification of the third embodiment.

Fig. 45 is a diagram showing a cross section of
15 the chip capacitor.

Fig. 46 is a diagram showing a cross section according to a fourth modification of the third embodiment.

Fig. 47 is a diagram showing a cross section of
20 the chip capacitor according to the fourth modification.

Fig. 48 is a diagram showing a process for manufacturing a printed circuit board according to a fourth embodiment of the present invention.

Fig. 49 is a diagram showing a process for
25 manufacturing a printed circuit board according to a fourth embodiment.

Fig. 50 is a diagram showing a process for manufacturing a printed circuit board according to a fourth embodiment.

30 Fig. 51 is a diagram showing a cross section of the printed circuit board according to a fourth embodiment.

Fig. 52 is a diagram showing a cross section of

the printed circuit board according to a fourth embodiment.

Fig. 53 is a diagram showing a cross section of the printed circuit board according to a first
5 modification of the fourth embodiment.

Fig. 54 is a diagram showing a cross section of the printed circuit board according to a second modification of the fourth embodiment.

Fig. 55 is a diagram showing a cross section of
10 the printed circuit board according to a third modification of the fourth embodiment.

Fig. 56 is a diagram showing a cross section of the printed circuit board according to a fourth modification of the fourth embodiment.

Fig. 57 is a diagram showing a cross section of
15 the printed circuit board according to a fifth modification of the fourth embodiment.

Fig. 58 is a diagram showing a cross section of the printed circuit board according to a sixth
20 modification of the fourth embodiment.

Fig. 59 is a diagram showing a cross section of the chip capacitor according to the sixth modification.

Fig. 60 is a diagram showing a process for manufacturing a printed circuit board according to a
25 fifth embodiment of the present invention.

Fig. 61 is a diagram showing a process for manufacturing a printed circuit board according to a fifth embodiment.

Fig. 62 is a diagram showing a process for
30 manufacturing a printed circuit board according to a fifth embodiment.

Fig. 63 is a diagram showing a cross section of the printed circuit board according to a fifth

embodiment.

Fig. 64 is a diagram showing a cross section of the printed circuit board according to a fifth embodiment.

5 Fig. 65 is a diagram showing a cross section of the printed circuit board according to a first modification of the fifth embodiment.

Fig. 66 is a diagram showing a cross section of the chip capacitor according to the first modification.

10 Fig. 67 is a diagram showing a cross section of the printed circuit board according to a second modification of the fifth embodiment.

Fig. 68 is a diagram showing a cross section of the chip capacitor according to the second modification.

15 Fig. 69 is a diagram showing a cross section of the printed circuit board according to a third modification of the fifth embodiment.

Fig. 70 is a diagram showing a cross section of the printed circuit board according to a fourth modification of the present invention.

20 Fig. 71 is a diagram showing a cross section of the printed circuit board according to a fifth modification.

Fig. 72 is a diagram showing a cross section according to a sixth modification.

Fig. 73 is a diagram illustrating a loop inductance of a printed circuit board according to a conventional technique.

30 Best Mode for Carrying Out the Invention (First Embodiment)

Hereinafter, embodiments of the present invention will be described with reference to the

drawings.

First, the structure of a printed circuit board according to a first embodiment of the present invention will be described with reference to Figs. 7 and 8. Fig. 7 is a diagram showing a cross section of a printed circuit board 10. Fig. 8 is a diagram showing a state where an IC chip 90 is mounted on the printed circuit board 10 shown in Fig. 7, and the printed circuit board 10 is attached onto a daughter board 95.

As shown in Fig. 7, the printed circuit board 10 is constituted by a core substrate 30 accommodating a plurality of chip capacitors 20, and a buildup circuit layers 80A, 80B. The buildup circuit layers 80A and 80B are constituted by an interlayer resin insulating layer 50 and 150. The interlayer resin insulating layer 50 has via holes 160 and conductor circuits 158. The interlayer resin insulating layer 150 has via holes 161 and conductor circuits 159. A solder resist layer 70 is formed on the interlayer resin insulating layer 150.

As shown in Fig. 17(A), the chip capacitor 20 is constituted by a first electrode 21, a second electrode 22, and a dielectric body 23 interposed between the first and second electrodes 21, 22. The dielectric body 23 includes a plurality of first conductive films 24 connected to the first electrode 21 and a plurality of second conductive films 25 connected to the second electrode 22 in an opposed relation to each other.

As shown in Fig. 8, a solder bump 76U is formed in each via hole 161 on the upper buildup circuit layer 80A to connect the buildup circuit layer 80A to each pad 92 of the IC chip 90. On the other hand, a solder bump 76D is formed in each via hole 161 on the lower buildup circuit layer 80B to connect the lower buildup circuit

layer 80B to each pad 94 of the daughter board 95. Through holes 46 are formed in the core substrate 30.

In this embodiment, the printed circuit board 10 is formed with a large cavity 32. Due to this structure, a plurality of chip capacitors 20 can reliably be arranged on the substrate even if the accuracy of spot-facing process is low. The chip capacitors 20 can be arranged in positions close to each other in the cavity 32, thereby increasing the packaging density of the capacitors. In addition, the plurality of chip capacitors 20 are arranged at identical heights to each other in the cavity 32, and therefore, as will be described later, the resin layer can be formed on the core substrate into a uniform thickness, and the via holes can be stably formed. Since the interlayer resin insulating layers 50, 150, and the conductor circuits 158, 159 can be appropriately formed on the core substrate 30, the rate of generating defective printed circuit boards 10 can be lowered.

As the material of the core substrate, a resin material is used. For example, resin materials used for general printed circuit boards, such as base materials impregnated with glass epoxy resin and base materials impregnated with phenolic resin. It is impossible to use substrates made of ceramic and AlN as the core substrate. These substrates are poor in outer shape processing characteristics, and cannot accommodate capacitors in some cases. In addition, a void is created inside the substrate even if it is filled with a resin.

Since a resin layer 36 is charged into the space between the chip capacitors 20, the chip capacitors 20 can be located and firmly fixed at accurate positions in the cavity 32. In addition, the migration at the connection between the capacitors and the via holes can

be prevented.

The thermal expansion coefficients of the resin layer 36 and the adhesive material 34 provided on the bottom surface of the chip capacitor 20 are set to the values lower than those of the core substrate 30 and the resin insulating layer 40, that is, are set to the values close to that of the chip capacitor 20 made of ceramics. In this manner, even if internal stress is generated between the core substrate 30 and the resin insulating layer 40, and the chip capacitors 20 caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings on the core substrate 30 and the resin insulating layer 40 do not easily occur. As a result, high reliability can be attained.

Since the resin layer 36 provided between the chip capacitors 20 has the through holes 46, a signal line does not pass through the chip capacitors 20 made of ceramics. This structure eliminates the problems that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body. It is possible to provide wires under the capacitors, and external terminals such as wires and pins have an increased degree of freedom, thereby attaining high density and small size.

As shown in Fig. 17(A), in the chip capacitor 20, the first electrode 21 and second electrode 22 respectively include a metal layer 26 and a copper plated film 29 coating the metal layer 26. The plated film is formed by electrolytic plating, electroless plating, and the like. As shown in Fig. 7, an electric connection for the first and second electrodes 21, 22 coated with the copper plated film 29 is established by the via hole

60 made of copper plating. The electrodes 21, 22 of the chip capacitor are metallized and has pits and projections on their surfaces. If the metal layer 26 is left uncoated and exposed to the outside, the resin may be left in the pits and projections in the step of forming openings 48 in the resin insulating layer 40 which will be described later. The resin left in the pits and projections may cause a disconnection between the first and second electrodes 21, 22 and the via hole 60.

Contrary to this, in the embodiment of the present invention, the surfaces of the first and second electrodes 21, 22 coated with the copper plated film 29 are flat and smooth. When the openings 48 are formed in the resin insulating layer 40 formed on the electrodes 21, 22, no resin is left on the surfaces of the electrodes 21, 22. When the via holes 60 are formed, the connection between the via holes 60 and the electrodes 21, 22 has increased reliability.

Since the via holes 60 are made by plating into the electrodes 21, 22 formed with the copper plated film 29, the electrodes 21, 22 are firmly connected to the via holes 60. No disconnection occurs between the electrodes 21, 22 and via holes 60 even when a heat cycle test is conducted.

The copper plated film 29 is formed after a nickel/tin layer provided onto the surface of the metal layer 26 in the step of manufacturing the chip capacitor is peeled off at the time of mounting the chip capacitor onto the printed circuit board. Alternatively, the copper plated film 29 may be directly provided onto the surface of the metal layer 26 in the step of manufacturing the chip capacitor 20. In this embodiment, openings which extend to the copper plated film 29 of the electrodes

is formed by a laser, and then a desmear process is performed to form via holes by copper plating. Therefore, even if an oxide film is formed on the surface of the copper plated film 29, the oxide film can be removed in the laser or desmear process. In this manner, the first and second electrodes 21, 22 can be properly connected to the via holes 60.

As shown in Fig. 17(B), the first and second electrodes 21, 22 of the capacitor 20 may be partially uncoated with the coating 28. When partially uncoated and exposed to the outside, the connection of the first and second electrodes 21, 22 to the via holes 60 can be enhanced.

On the surface of the dielectric body 23 made of ceramic of the chip capacitor 20, a rough surface 23 α may be formed. The rough surface 23 α contributes to an increased adhesion between the chip capacitor 20 made of ceramic and a resin insulating layer 40 made of resin, thereby avoiding the resin insulating layer 40 from peeling from the interface with the chip capacitor 20 even when a heat cycle test is conducted. The rough surface 23 α can be formed by polishing the surface of the chip capacitor 20 after the sintering step, or by roughening the surface of the chip capacitor 20 before the sintering step. In this embodiment, the surface of the chip capacitor is roughened to increase its adhesion with the resin insulating layer. Alternatively, the surface of the chip capacitor may be subjected to silane coupling process.

Next, the method for manufacturing the printed circuit board, described above with reference to Fig. 7, will be described with reference to Figs. 1 to 7.

(1) First, a core substrate 30 which is an insulating resin substrate is used as a starting material (Fig. 1(A)). Then, a cavity 32 for accommodating capacitors is formed on one side of the core substrate 30 by a spot-facing process (Fig. 1(B)). At this time, the cavity 32 is formed to have an area larger than the area in which a plurality of capacitors are to be provided. In this manner, a plurality of capacitors can be provided on the core substrate 30 assuredly.

(2) After that, an adhesive material 34 is applied onto the cavity 32 by a printer (Fig. 1(C)). At this time, potting may be conducted on top of the application of the adhesive material 34. As the adhesive material 34, an adhesive material having a thermal expansion coefficient smaller than those of the core substrate 30 and the resin insulating layer 40 is used. Then, a plurality of chip capacitors 20 (Fig. 17) made of ceramic are placed onto the adhesive material 34 (Fig. 1(D)). By placing a plurality of chip capacitors 20 onto the cavity 32 having a flat and smooth bottom surface, the plurality of chip capacitor 20 are aligned into the same heights with each other. Thus-obtained core substrate 30 has a flat and smooth surface. In addition, since the cavity 32 has a large area, the chip capacitors 20 can be located at accurate positions with high density.

(3) The top surfaces of the chip capacitors 20 are pushed or tapped to align the chip capacitors 20 into the same heights with each other (Fig. 2(A)). By this process, even if chip capacitors 20 having largely different sizes from each other are provided in the cavity 32, they are aligned into the completely same heights with each other. As a result, the core substrate 30 can has a flat and smooth surface.

(4) After that, a thermosetting resin is charged into the space between the chip capacitors 20 in the cavity 32, and then is heated and cured to form a resin layer 36 (Fig. 2(B)). The thermosetting resin is preferably selected from the group consisting of epoxy, phenol, polyimide, and triazine. The resin layer 36 serves to fix the chip capacitors 20 in the cavity 32. For the resin layer 36, a resin having a thermal expansion coefficient smaller than those of the core substrate 30 and the resin insulating layer 40 is used.

Alternatively, the resin layer 36 may be made of other resins such as thermoplastic resin. The resin may be impregnated with a filler for adjusting the thermal expansion coefficient. Examples of the filler include inorganic fillers, ceramic fillers, and metal fillers.

(5) Onto thus-obtained structure, a resin selected from epoxy resins which will be described later is applied with a printer to form a resin insulating layer 40 (Fig. 2(C)). Instead of applying the resin, a resin film may be attached.

Instead of epoxy resins, it is also possible to use one or more resins selected from the group consisting of thermosetting resins, thermoplastic resins, photosensitive resins, complexes of thermosetting resins and thermoplastic resins, and complexes of photosensitive resins and thermoplastic resins. The resin insulating layer may have two-layered structure made of these resins.

(6) After that, openings 48 for via holes are formed in the resin insulating layer 40 by a laser (Fig. 2(D)), and then, a desmear process is conducted. Instead of the process using a laser, exposure to light and development may be employed. Then, penetrating

openings 46a for through holes are formed with a drill or laser, and are heated and cured (Fig. 3(A)).

Alternatively, a desmear process using a drug solution of permagnetic acid or plasma may be conducted.

5 (7) A copper plated film 52 is formed on the surface of the resin insulating layer 40 by an electroless copper plating (Fig. 3(B)). Instead of the electroless plating to form the copper plated film 52, it is also possible to conduct sputtering using an Ni-Cu alloy as a target
10 to form an Ni-Cu alloy layer. As the case may be, after the sputtering to form the Ni-Cu alloy layer, an electroless plated film may be formed thereon.

(8) A photosensitive dry film is attached on the surface of the copper plated film 52, and a mask is placed
15 thereon. In this state, exposure to light and development are conducted to form a resist 54 having a predetermined pattern. The resultant core substrate 30 is immersed into an electrolytic plating solution, and a current is allowed to flow into the core substrate 30
20 through the copper plated film 52 to precipitate an electrolytic plated film 56 (Fig. 3(C)).

(9) The plated resist 54 is peeled and removed with 5% NaOH, and the copper plated film 52 located under the plated resist 54 is etched with a mixed solution of
25 sulfuric acid and hydrogen peroxide to be dissolved and removed. As a result, a conductor circuit 58 (including via holes 60) constituted by the copper plated film 52 and the electrolytic copper plated film 56, and through holes 46 are formed. Since the through holes 46 are
30 formed, no signal line passes through the chip capacitors 20. In this manner, there is no problem that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission

is delayed by passing through the high dielectric body. An etching solution is sprayed onto both surfaces of the substrate to etch the surface of the conductor circuit 58 and the land surfaces of the through holes 46 to form
5 a rough surface 58 α over the entire surface of the conductor circuit 58 (Fig. 3(D)).

(10) A resin filler 62 containing epoxy resin as a main component is charged into the through holes 46, and is dried (Fig. 4(A)). Instead of the resin filler
10 containing epoxy resin as a main component, it is also possible to use thermosetting resins, thermoplastic resins, and UV ray hardening resins. Among them, thermosetting resins are preferable, because they are easy to handle when charged into the through holes.

(11) After the foregoing process is finished, a thermosetting epoxy resin sheet having a thickness of 50 μ m is vacuum-seal laminated to both surfaces of the substrate while raising the temperature in a range
15 between 50 and 150°C under a pressure of 5kg/cm² to form an interlayer resin insulating layer 50 made of epoxy resin (Fig. 4(B)). The degree of vacuum when the vacuum
20 sealing process is performed is 10mmHg. Instead of epoxy resin, olefin resin also may be used.

(12) Openings 148 each having a diameter of 80
25 μ m for via holes are formed in the interlayer resin insulating layer 50 with a CO² gas laser having a wavelength of 10.4 μ m under conditions that the beam diameter is 5mm, the mode is the top-hat mode, the pulse
width is 5.0 μ second, the hole diameter of mask is 0.5mm,
30 and three shots are performed (Fig. 4(C)). Then, a desmear process is conducted using an oxygen plasma.

(13) A plasma treatment is conducted using SV-4540 manufactured by Nippon Shinku Gijyutsu Co., Ltd. where the surface of the interlayer resin insulating layer 50 is roughen to form a rough surface 50 α (Fig. 4(D)). The plasma treatment is conducted using an argon as an inert gas with an electric power of 200W under gas pressure of 0.6Pa at 70°C for 2 minutes. Instead of the plasma treatment, roughening process may be conducted using an acid or oxidizer. The rough surface preferably has a thickness of 0.1 to 5 μ m.

(14) The argon gas in the SV-4540 is exchanged with new argon gas, and the sputtering is conducted using an Ni-Cu alloy as a target in the same SV-4540 with an electric power of 200W under a pressure of 0.6Pa at 80°C for 5 minutes to form an Ni-Cu alloy layer 152 on the surface of the interlayer resin insulating layer 50. The Ni-Cu alloy layer 152 has a thickness of 0.2 μ m (Fig. 5(A)). Alternatively, a plated film such as an electroless plated film may be formed, or a plated film may be formed on the sputtered Ni-Cu alloy layer 152.

(15) After the foregoing steps, a commercially available photosensitive dry film is attached on both sides of the substrate 30, and a photo mask film is placed thereon. In this state, the substrate 30 is exposed to light with 100mJ/cm². Then, the substrate 30 is developed with 0.8% sodium carbonate to form a plated resist 154 having a thickness of 15 μ m. After that, an electrolytic plating is conducted under the following conditions to form an electrolytic plated film 156 having a thickness of 15 μ m (Fig. 5(B)). By this process, the electrolytic plated film 156 enlarges the thickness of

the portion which will be the conductor circuit 158 in the step described later and fills and plates the portion which will be the via holes 160 in the steps described later. The additive added in the electrolytic plating aqueous solution is Caparaside HL produced by Atotech Japan Co., Ltd.

[Electrolytic plating aqueous solution]

sulfuric acid: 2.24mol/l

copper sulfate: 0.26mol/l

additive (Caparaside HL produced by Atotech Japan Co., Ltd.): 19.5mol/l

[Conditions for electrolytic plating]

current density: 1A/dm²

time: 65 minutes

temperature 22±2°C

(16) The plated resist 154 is peeled and removed in 5% NaOH. After that, the Ni-Cu alloy layer 152 located under the plated resist is dissolved and removed by etching using sulfuric acid and a mixed solution of sulfuric acid and hydrogen peroxide. As a result, a conductor circuit 158 having a thickness of 16 μm constituted by the Ni-Cu alloy layer 152 and the electrolytic plated film 156, and via holes 160 (Fig. 5(C)).

(17) The foregoing steps (11) to (16) are repeated to further forming an upper interlayer resin insulating layer 150 and a conductor circuit 159 (including via holes 161) (Fig. 5(D)).

(18) Into a vessel, added are 46.67 parts by weight of oligomer which is obtained by forming 50% of epoxy groups of 60 weight percent cresol novolac epoxy resin (manufactured by Nippon Kayaku) dissolved in diethylene

glycol dimethyl ether (DMDG) into an acrylic structure and which imparts photosensitive characteristic, 15 parts by weight of 80 weight percent bisphenol A epoxy resin (Epicoat 1001 manufactured by Yuka Shell) dissolved in methylethyl ketone, 1.6 parts by weight of imidazole hardening agent (2E4MZ-CN manufactured by Shikoku Chemical), 3 parts by weight of polyhydric acryl monomer which is a photosensitive monomer (R604 manufactured by Kyoei Chemical), 1.5 parts by weight of polyhydric acryl monomer (DEP6A manufactured by Kyoei Chemical), and 0.71 parts by weight of dispersing defoaming agent (S-65 manufactured by Sannopuko), and mixed and stirred with one another to prepare a mixed composition. Into the mixed composition, added are 2.0 parts by weight of benzophenone (manufactured by Kanto Chemical) serving as a photoinitiator, and 0.2 parts by weight of Michler's ketone (manufactured by Kanto Chemical) serving as a photosensitizer. Then, the viscosity is adjusted to 2.0 Pa·s at 25°C so that a solder resist composition (i.e. an organic resin insulating material) is obtained.

The viscosity is measured by using No. 4 rotor of a B-type visometer (DVL-B manufactured by Tokyo Keiki) when the velocity is 60 rpm and No. 3 rotor of the same when the velocity is 6 rpm.

(19) The solder resist composition is applied to both surfaces of the substrate 30 to have a thickness of 20 μ m, and is dried at 70°C for 20 minutes and 70°C for 30 minutes. A photomask having a thickness of 5mm on which a pattern of the solder resist openings are drawn is made hermetic contact and placed onto the solder resist layer 70, and is exposed to light with 1000mJ/cm². Then, the resultant is developed with a DMTG solution to form

openings 71U, 71D each having a diameter of $200\text{ }\mu\text{m}$ (Fig. 6(A)). Alternatively, a commercially available solder resist such as LPSR may be employed.

(20) The substrate formed with the solder resist layer (i.e. organic resin insulating layer) 70 is immersed into an electroless nickel plating solution containing nickel chloride ($2.3\times 10^{-1}\text{mol/l}$), sodium hypophosphite ($2.8\times 10^{-1}\text{mol/l}$), sodium citrate ($1.6\times 10^{-1}\text{mol/l}$) and having pH of 4.5 for 20 minutes to form a nickel plated layer 72 having a thickness of $5\text{ }\mu\text{m}$ in the openings 71U, 71D. The resultant substrate is immersed into an electroless plating solution containing gold potassium cyanide ($7.6\times 10^{-3}\text{mol/l}$), ammonia chloride ($1.9\times 10^{-1}\text{mol/l}$), sodium citrate ($1.2\times 10^{-1}\text{mol/l}$), and sodium hypophosphite ($1.7\times 10^{-1}\text{mol/l}$) at 80°C for 7.5 minutes to form a gold plated layer 74 having a thickness of $0.03\text{ }\mu\text{m}$ on the nickel plated layer 72. In this manner, solder pads 75 are formed in the via holes 161 and the conductor circuit 159 (Fig. 6(B)).

(21) A solder paste is printed in the openings 71U, 71D of the solder resist layer 70, and is reflowed at 200°C to form solder bumps (solder bodies) 76U, 76D. In this manner, the printed circuit board 10 having the solder bumps 76U, 76D is obtained (Fig. 7).

Next, a method for mounting an IC chip onto the printed circuit board 10 obtained in the foregoing steps, and a method for attaching the printed circuit board 10 onto a daughter board will be described with reference to Fig. 8. An IC chip 90 is placed on the printed circuit board 10 in such a manner that the solder pads 92 of the IC chip 90 corresponds to the solder bumps 76U of the

printed circuit board 10, and is reflowed. As a result, the IC chip 90 is mounted on the printed circuit board 10. Similarly, the printed circuit board 10 is placed on the daughter board 95 in such a manner that the pads 5 94 of the daughter board 95 corresponds to the solder bumps 76D of the printed circuit board 10, and is reflowed. As a result, the printed circuit board 10 is attached to the daughter board 95.

The above-described resin film contains a
10 refractory resin, soluble particles, a hardening agent, and other components. Hereinafter, each of them will be described.

The resin film used in the manufacturing method of the present invention has a structure in that particles
15 soluble in acid or an oxidizer (hereinafter, referred to as "soluble particles") are dispersed in resin which is refractory with respect to acid or an oxidizer (hereinafter, referred to as "refractory resin").

The expressions "refractory" and "soluble" will
20 now be described. When materials are immersed in solution composed of the same acid or the same oxidizers for the same time, a material of a type which is dissolved at a relatively high dissolving rate is called a "soluble" material for convenience. A material of a type which
25 is dissolved at a relatively slow dissolving rate is called a "refractory material" for convenience.

The soluble particles are exemplified by resin particles which are soluble in acid or an oxidizer (hereinafter called "soluble resin particles"),
30 inorganic particles which are soluble in acid or an oxidizer (hereinafter called "inorganic soluble particles") and metal particles which are soluble in acid or an oxidizer (hereinafter called "soluble metal

particles"). The foregoing soluble particles may be employed solely or two or more particles may be employed.

The shape of each of the soluble particles is not limited. The shape may be a spherical shape or a pulverized shape. It is preferable that the particles have a uniform shape. The reason for this lies in that a rough surface having uniformly rough pits and projections can be formed.

It is preferable that the mean particle size of the soluble particles is $0.1\mu\text{m}$ to $10\mu\text{m}$. When the particles have the diameters satisfying the foregoing range, particles having two or more particle sizes may be employed. That is, soluble particles having a mean particle size of $0.1\mu\text{m}$ to $0.5\mu\text{m}$ and soluble particles having a mean particle size of $1\mu\text{m}$ to $3\mu\text{mm}$ may be mixed. Thus, a more complicated rough surface can be formed. Moreover, the adhesiveness with the conductor circuit can be improved. In the present invention, the particle size of the soluble particles is the length of a longest portion of each of the soluble particles.

The soluble resin particles may be particles constituted by thermosetting resin or thermoplastic resin. When the particles are immersed in solution composed of acid or an oxidizer, the particles must exhibit dissolving rate higher than that of the foregoing refractory resin.

Specifically, the soluble resin particles are exemplified by particles constituted by epoxy resin, phenol resin, polyimide resin, polyphenylene resin, polyolefin resin or fluorine resin. The foregoing material may be employed solely or two or more materials may be mixed.

The soluble resin particles may be resin particles constituted by rubber. Rubber above is exemplified by polybutadiene rubber, a variety of denatured polybutadiene rubber, such as denatured epoxy rubber, denatured urethane rubber or denatured (metha) acrylonitrile rubber, and (metha) acrylonitrile butadiene rubber containing a carboxylic group. When the foregoing rubber material is employed, the soluble resin particles can easily be dissolved in acid or an oxidizer. That is, when the soluble resin particles are dissolved with acid, dissolution is permitted with acid except for strong acid. When the soluble resin particles are dissolved, dissolution is permitted with permanganate which has a relatively weak oxidizing power. When chromic acid is employed, dissolution is permitted even at a low concentration. Therefore, retention of the acid or the oxidizer on the surface of the resin can be prevented. When a catalyst, such as palladium chloride, is supplied after the rough surface has been formed as described later, inhibition of supply of the catalyst and oxidation of the catalyst can be prevented.

The inorganic soluble particles are exemplified by particles made of at least a material selected from a group consisting of an aluminum compound, a calcium compound, a potassium compound, a magnesium compound and a silicon compound.

The aluminum compound is exemplified by alumina and aluminum hydroxide. The calcium compound is exemplified by calcium carbonate and calcium hydroxide. The potassium compound is exemplified by potassium carbonate. The magnesium compound is exemplified by magnesia, dolomite and basic magnesium carbonate. The silicon compound is exemplified by silica and zeolite.

The foregoing material may be employed solely or two or more materials may be mixed.

The soluble metal particles are exemplified by particles constituted by at least one material selected from a group consisting of copper, nickel, iron, zinc, lead, gold, silver, aluminum, magnesium, potassium and silicon. The soluble metal particles may have surfaces coated with resin or the like in order to maintain an insulating characteristic.

When two or more types of the soluble particles are mixed, it is preferable that the combination of the two types of soluble particles is combination of resin particles and inorganic particles. Since each of the particles has low conductivity, an insulating characteristic with the resin film can be maintained. Moreover, the thermal expansion can easily be adjusted with the refractory resin. Thus, occurrence of a crack of the interlayer resin insulating layer constituted by the resin film can be prevented. Thus, separation between the interlayer resin insulating layer and the conductor circuit can be prevented.

The refractory resin is not limited when the resin is able to maintain the shape of the rough surface when the rough surface is formed on the interlayer resin insulating layer by using acid or oxidizer. The refractory resin is exemplified by thermosetting resin, thermoplastic resin and their composite material. As an alternative to this, the foregoing photosensitive resin of a type having photosensitive characteristic imparted thereto may be employed. When the photosensitive resin is employed, exposure and development processes of the interlayer resin insulating layers can be performed to form the openings for the via

holes.

In particular, it is preferable that the resin containing thermosetting resin is employed. In the foregoing case, the shape of the rough surface can be maintained against plating solution and when a variety of heating processes are performed.

The refractory resin is exemplified by epoxy resin, phenol resin, phenoxy resin, polyimide resin, polyphenylene resin, polyolefin resin and fluorine resin. The foregoing material may be employed solely or two or more types of the materials may be mixed.

It is preferable that epoxy resin having two or more epoxy groups in one molecule thereof is employed. The reason for this lies in that the foregoing rough surface can be formed. Moreover, excellent heat resistance and the like can be obtained. Thus, concentration of stress onto the metal layer can be prevented even under a heat cycle condition. Thus, occurrence of separation of the metal layer can be prevented.

The epoxy resin is exemplified by cresol novolac epoxy resin, bisphenol-A epoxy resin, bisphenol-F epoxy resin, phenol novolac epoxy resin, alkylphenol novolac epoxy resin, biphenol-F epoxy resin, naphthalene epoxy resin, dicyclopentadiene epoxy resin, an epoxy material constituted by a condensation material of phenol and an aromatic aldehyde having a phenol hydroxyl group, triglycidyl isocyanurate and alicyclic epoxy resin. The foregoing material may be employed solely or two or more material may be mixed. Thus, excellent heat resistance can be realized.

It is preferable that the soluble particles in the resin film according to the present invention are

substantially uniformly dispersed in the refractory resin. The reason for this lies in that a rough surface having uniform pits and projections can be formed. When via holes and through holes are formed in the resin film, adhesiveness with the metal layer of the conductor circuit can be maintained. As an alternative to this, a resin film containing soluble particles in only the surface on which the rough surface is formed may be employed. Thus, the portions of the resin film except for the surface is not exposed to acid or the oxidizer. Therefore, the insulating characteristic between conductor circuits through the interlayer resin insulating layer can reliably be maintained.

It is preferable that the amount of the soluble particles which are dispersed in the refractory resin is 3 wt% to 40 wt% with respect to the resin film. When the amount of mixture of the soluble particles is lower than 3 wt%, the rough surface having required pits and projections cannot be formed. When the amount is higher than 40 wt%, deep portions of the resin film are undesirably dissolved when the soluble particles are dissolved by using acid or the oxidizer. Thus, the insulating characteristic between the conductor circuits through the interlayer resin insulating layer constituted by the resin film cannot be maintained. Thus, short circuit is sometimes caused to occur.

It is preferable that the resin film contains a hardening agent and other components as well as the refractory resin.

The hardening agent is exemplified by an imidazole hardening agent, an amine hardening agent, a guanidine hardening agent, an epoxy adduct of each of the foregoing hardening agents, a microcapsule of each of the foregoing

hardening agents and an organic phosphine compound, such as triphenylphosphine or tetraphenyl phosphonium tetraphenyl borate.

It is preferable that the content of the hardening agent is 0.05 wt% to 10 wt% with respect to the resin film. When the content is lower than 0.05 wt%, the resin film cannot sufficiently be hardened. Thus, introduction of acid and the oxidizer into the resin film occurs greatly. In the foregoing case, the insulating characteristic of the resin film sometimes deteriorates. When the content is higher than 10 wt%, an excessively large quantity of the hardening agent component sometimes denatures the composition of the resin. In the foregoing case, the reliability sometimes deteriorates.

The other components are exemplified by an inorganic compound which does not exert an influence on the formation of the rough surface and a filler constituted by resin. The inorganic compound is exemplified by silica, alumina and dolomite. The resin is exemplified by polyimide resin, polyacrylic resin, polyamideimide resin, polyphenylene resin, melanine resin and olefin resin. When any one of the foregoing fillers is contained, conformity of the thermal expansion coefficients can be established. Moreover, heat resistance and chemical resistance can be improved. As a result, the performance of the printed circuit board can be improved.

The resin film may contain solvent. The solvent is exemplified by ketone, such as acetone, methylethylketone or cyclohexane; aromatic hydrocarbon, such as ethyl acetate, butyl acetate, cellosolve acetate, toluene or xylene. The foregoing material may be employed solely or two or more materials may be mixed.

(First Modification of First Embodiment)

A printed circuit board 110 according to a first modification of the first embodiment of the present invention will be described with reference to Fig. 15. In the foregoing first embodiment, the BGA is provided. The first modification of the first embodiment has a structure similar to that according to the first embodiment, except that a PGA method is employed with which connection is established through conductive connection pins 96 as shown in Fig. 15.

A method for manufacturing the printed circuit board described above with reference to Fig. 15 will be described referring to Figs. 9 to 15.

(1) Four prepregs 33 impregnated with an epoxy resin are laminated on top of each other to form a laminated plate 31a, and a penetrating opening 37a for accommodating chip capacitors is formed in the laminated plate 31a. On the other hand, two prepregs 33 are laminated on top of each other to form a laminated plate 31b (Fig. 9(A)). The prepreg 33 may be impregnated with, instead of the epoxy resin, BT, phenolic resin, or reinforcement material such as glass cloth.

By forming the penetrating opening 37a for accommodating chip capacitors in such a manner as to have a large area, a plurality of chip capacitors 20 can be accommodated in a cavity 37 assuredly in the step described later.

(2) The laminated plates 31a and 31b are vacuum-seal laminated to each other, and are heated and cured. As a result, a core substrate 31 formed with the cavity 37 capable of accommodating a plurality capacitors 20 is obtained (Fig. 9(B)).

(3) An adhesive material 34 is applied with a printer to positions on the cavity 37 where the capacitors 20 will be mounted. Then, a plurality of chip capacitors 20 made of ceramic are accommodated in the cavity 37 via the adhesive material 34 (Fig. 9(C)). By placing a plurality of chip capacitors 20 in the cavity 37, the plurality of chip capacitor 20 are aligned into the same heights with each other. Thus-obtained core substrate 31 has a flat and smooth surface. In addition, since the cavity 37 has a large area, the chip capacitors 20 can be located at accurate positions with high density. In this manner, a resin layer can be formed on the core substrate into a uniform thickness, thereby properly forming via holes in the core substrate 31 as will be described later. As a result, the rate of generating defective printed circuit boards can be lowered.

(4) The top surfaces of the chip capacitors 20 are pushed or tapped to align the chip capacitors 20 into the same heights with each other (Fig. 9(D)). By this process, even if chip capacitors 20 having largely different sizes from each other are provided in the cavity 37, they are aligned into the completely same heights with each other. As a result, the core substrate 31 can has a flat and smooth surface.

(5) After that, a thermosetting resin is charged into the space between the chip capacitors 20 in the cavity 37, and then is heated and cured to form a resin layer 36 (Fig. 10(A)). The thermosetting resin is preferably selected from the group consisting of epoxy, phenol, polyimide, and triazine. In this manner, the chip capacitors 20 can be fixed in the cavity 37.

(6) Onto thus-obtained structure, a resin selected from the above-described epoxy resins and

polyolefin resins is applied with a printer to form a resin insulating layer 40 (Fig. 10(B)). Instead of applying the resin, a resin film may be attached.

(7) After that, openings 48 for via holes are formed in the resin insulating layer 40 by exposure to light and development or a laser (Fig. 10(C)). Then, penetrating openings 46a for through holes are formed in the resin layer 36 with a drill or a laser, and the resin layer 36 is heated and dried (Fig. 10(D)).

(8) A palladium catalyst is provided to the substrate 31, and then, the core substrate is immersed into an electroless plating solution to uniformly precipitate an electroless plated film 53 (Fig. 11(A)). In the foregoing case, an electroless plating is employed. As an alternative to this, a metal layer of copper, nickel and the like may be formed by sputtering. As the case may be, an electroless plated film may be formed on the metal layer after the formation of the metal layer by sputtering.

(9) A photosensitive dry film is attached on the surface of the electroless plated film 53, and a mask is placed thereon. In this state, exposure to light and development are conducted to form a resist 54 having a predetermined pattern. The resultant core substrate 31 is immersed into an electrolytic plating solution, and a current is allowed to flow into the core substrate 31 through the electroless plated film 53 to precipitate the electrolytic plated film 56 (Fig. 11(B)).

(10) After the foregoing processes, the resist 54 is peeled and removed with 5% NaOH, and the copper plated film 53 located under the plated resist 54 is etched with a mixed solution of sulfuric acid and hydrogen peroxide to be dissolved and removed. As a result, a

conductor circuit 58 (including via holes 60)
constituted by the electroless plated film 53 and the
electrolytic copper plated film 56, and through holes
46 are formed. Since the through holes 46 are formed,
5 no signal line passes through the chip capacitors 20.
In this manner, there is no problem that the impedance
becomes discontinuous by the high dielectric body to
generate a reflection, and that the transmission is
delayed by passing through the high dielectric body.

10 (11) The substrate 31 is cleaned with water and
is degreased with acid, and then, is subjected to soft
etching. After that, etching solution is sprayed to both
surfaces of the substrate 31 so that the surface of the
conductor circuit 58 and the surface of each land of each
15 through hole 46 are etched. Thus, a rough surface 58
 α is formed over the entire surface of the conductor
circuit 58 (Fig. 11(C)). The etching solution is mixed
solution of 10 parts by weight of copper (II) imidazole
complex, 7 parts by weight of glycolic acid, and 5 parts
20 by weight of potassium chloride (Mech etch bond,
manufactured by Mech Co., Ltd.).

(12) Into a container, added are 100 parts by
weight of bisphenol-F epoxy monomer (YL983U having a
molecular weight of 310, manufactured by Yuka Shell),
25 170 parts by weight of SiO₂ spherical particles
(CRS1101-CE manufactured by Adotech) having surfaces
each of which is coated with a silane coupling agent and
a mean particle size of 1.6 μ m and structured such that
the diameter of the largest particle is 15 μ m or smaller,
30 and 1.5 parts by weight of leveling agent (Pelenol S4
manufactured by Sannopuko). These materials are
stirred and mixed to prepare a resin filler 62 having

a viscosity of 45 to 49Pa's at $23\pm 1^{\circ}\text{C}$. As a hardening agent, 6.5 parts by weight of imidazole hardening agent (2E4MZ-CN manufactured by Shikoku Kasei) is employed.

5 The resin filler 62 is charged into each through hole 46, and is dried (Fig. 11(D)).

(13) 30 parts by weight of bisphenol-A epoxy resin (Epicoat 1001 having an epoxy equivalent of 469, manufactured by Yuka Shell), 40 parts by weight of cresol novolac epoxy resin (Epichron N-673 having an epoxy
10 equivalent of 215, manufactured by Dainippon Ink & Chremicals), 30 parts by weight of phenol novolac resin containing a triazine structure (Phenolight KA-7052 having a phenol hydroxyl group equivalent of 120, manufactured by Dainippon Ink & Chemicals) are heated
15 and dissolved in 20 parts by weight of ethyldiglycol acetate and 20 parts by weight of solvent naphtha while being stirred. Then, 15 parts by weight of polybutadine rubber having epoxy terminal (Denalex R-45EPT manufactured by Nagase Chemicals), 1.5 parts by weight
20 of pulverized 2-phenyl-4, 5-bis(hydroxymethyl) imidazole, 2 parts by weight of particle-seize reduced silica, and 0.5 parts by weight of silicon defoaming agent are added to prepare 0.5 parts by weight of epoxy resin composition.

25 The obtained epoxy resin composition is applied onto a PET film having a thickness of $38\mu\text{m}$ using a roll coater such that the thickness after the PET film is dried is $50\mu\text{m}$. Then, drying is performed at 80 to 120°C for 10 minutes. Thus, a resin film for the interlayer resin
30 insulating layer is manufactured.

(14) Thus-manufactured resin film for the interlayer resin insulating layer is placed on the

substrate 31 manufactured in the above step (13). In this case, the resin film has a size slightly larger than the substrate 31. Then, temporal pressing is performed under conditions that the pressure is 4kgf/cm^2 , the temperature is 80°C , and the pressing duration is 10 seconds, and then, cutting is performed. After that, a vacuum laminator apparatus is operated to bond the resin film by the following method thereby forming an interlayer resin insulating layer 50 (Fig. 12(A)). That is, main pressing of the resin film for the interlayer resin insulating layer to the surface of the substrate 31 is performed under conditions that the degree of vacuum is 0.5 Torr, the pressure is 4kgf/cm^2 , the temperature is 80°C , and the pressing duration is 60 seconds. Then, curing with heat is performed at 170°C for 30 minutes.

(15) A mask 47 incorporating penetrating openings 47a formed therein and having a thickness of 1.2mm is placed on the interlayer resin insulating layer 50. Then, CO_2 gas laser beam having a wavelength of $10.4\ \mu\text{m}$ is used to form openings 148 for the via holes each having a diameter of $80\ \mu\text{m}$ are formed in the interlayer resin insulating layer 50 under conditions that the beam diameter is 4.0mm, the mode is the top-hat mode, the pulse width is $8.0\ \mu\text{sec}$, the diameter of each penetrating opening in the mask is 1.0mm, and one shot is performed (Fig. 12(B)).

(16) The substrate 31 formed with the openings 148 for the via holes is immersed in solution which contains 60g/l permanganic acid and has a temperature of 80°C for 10 minutes so as to dissolve and remove the epoxy resin particles present on the surface of the

interlayer resin insulating layer 50. As a result, the surface of the interlayer resin insulating layer 50 including the inner wall of each opening 148 for the via hole is roughened to be a rough surface 50 α (Fig. 12(C)).

5 Alternatively, the surface of the interlayer resin insulating layer 50 may be roughened with an acid or an oxidizer. The rough surface preferably has a thickness of 0.1 to 5 μ m.

(17) The substrate 31 after being subjected to
10 the foregoing process is immersed in neutral solution (manufactured by Siplay), and then cleaned with water. The surface of the substrate 31 subjected to the roughening process (depth of roughness is 3 μ m) is supplied with palladium catalyst. Thus, the catalyst
15 cores are adhered to the surface of the interlayer resin insulating layer 50 and the inner wall of each opening 48 for the via hole.

(18) The substrate is immersed into electroless copper plating solution having the following composition
20 to form an electroless copper plated film 153 having a thickness of 0.6 to 3.0 μ m over the entire surface of the rough surface 50 α (Fig. 12(D)).

NiSO₄: 0.003 mol/l

tartaric acid: 0.200 mol/l

25 copper sulfate: 0.030 mol/l

HCHO: 0.050 mol/l

NaOH: 0.100 mol/l

α ' α -bipyridyl: 40 mg/l

polyethylene glycol (PEG): 0.10 mg/l

30 [Electroless Plating Conditions]

40 minutes in a state where the temperature of

the solution is 35°C.

(19) A commercially available photosensitive dry film is bonded to the electroless copper plated film 153, and a mask is placed thereon. The resultant is subjected to exposure to light with 100mJ/cm², and is developed with 0.8% sodium carbonate to form a plating resist 154 having a thickness of 30 μm (Fig. 13(A)).

(20) The substrate 31 is cleaned with water of 50°C and is degreased. Then, the substrate 31 is cleaned with water of 25°C, and is further cleaned with sulfuric acid. After that, an electroplating is performed under the following conditions to form an electrolytic copper plated film 156 having a thickness of 20 μm (Fig. 13(B)).

[Electroplating solution]

sulfuric acid: 2.24mol/l

copper sulfate: 0.26 mol/l

additive: 19.5 ml/l

(Kapalacid HL, manufactured by Atotech Japan)

[Electroplating Conditions]

current density: 1A/dm²

duration: 65 minutes

temperature: 22 ± 2°C

(21) The plating resist 154 is peeled and removed with 5% NaOH, and then the electroless copper plated film 153 located under the plating resist 154 is dissolved and removed by performing etching using mixed solution of sulfuric acid and hydrogen peroxide. Thus, a conductor circuit 158 (including via holes 161) constituted by the electroless copper plated film 153 and the electrolytic copper plated film 156 and having a thickness of 18 μm is formed. After that, the same

process as the process (11) is conducted to form a rough surface 158 α with an etching solution containing cupric complex and an organic acid (Fig. 13(C)).

(22) The foregoing processes (14) to (21) are repeated to further forming an upper interlayer resin insulating layer 150 and a conductor circuit 159 (including via holes 161) (Fig. 13(D)).

(23) By repeating the process of the first embodiment, a solder resist composition (i.e. an organic resin insulating material) is obtained.

(24) The solder resist composition prepared in the foregoing process (23) is applied on both sides of the multi-layer printed circuit board into a thickness of 20 μ m. Then, the resultant is dried and exposed to UV ray, and is developed with a DMTG solution to form openings 71U, 71D each having a diameter of 200 μ m.

Then, a heat process is performed to cure the solder resist composition. As a result, a solder resist layer 70 having the openings 71U, 71D and a thickness of 20 μ m is formed (Fig. 14(A)). As the solder resist composition, it is also possible to use a commercially available solder resist composition.

(25) The substrate formed with the solder resist layer 70 is immersed into an electroless nickel plating solution of the same type as that used in the first embodiment to form a nickel plated layer 72 having a thickness of 5 μ m in the openings 71U, 71D. Thus-formed substrate is immersed into an electroless gold plating solution of the same type as that used in the first embodiment to form a gold plated layer 74 having a thickness of 0.03 μ m on the nickel plated layer 72 (Fig.

14(B)).

(26) A solder paste containing tin-lead is printed to each opening 71U in the solder resist layer 70 on the surface of the substrate on which the IC chip is to be mounted. Moreover, a solder paste as a conductive adhesive 97 is printed to each opening 71D on the other surface of the substrate. Conductive connection pins 96 are attached and held to a proper pin holding apparatus so that the fixing section 98 of each conductive connection pin 96 is brought into contact with the conductive adhesive 97 in the opening 71D. Then, reflowing is conducted to fix the fixing section 98 of each conductive connection pin 96 to the conductive adhesive 97. As a method for attaching the conductive connection pins 96, the conductive adhesive 97 is formed into the shape of ball, and is inserted into each opening 71D, or alternatively, the conductive adhesive 97 is bonded to each fixing section 98, and the conductive connection pins 96 are attached thereto. After that, reflowing may be conducted.

An IC chip 90 is mounted in such a manner that the solder pads 92 of the IC chip 90 corresponds to the solder bumps 76U on the side of openings 71U of the printed circuit board 110. Then, reflowing is conducted to attach the IC chip 90 to the printed circuit board 110 (Fig. 15).

(Second modification of First embodiment)

A method for manufacturing a printed circuit board according to a second modification of the first embodiment will be described with reference to Fig. 16.

(1) For prepregs 33 each of which is impregnated with epoxy resin are laminated and cured to form a laminated plate 31a. Through openings 37a for

accommodating chip capacitors are formed in the laminated plate 31a. On the other hand, a sheet 31c constituted by an uncured prepreg 33 and a plate 31b constituted by a cured prepreg 33 are prepared (Fig. 16(A)).

5 (2) The laminated plate 31a and the plate 31b are press-laminated to each other to form a substrate 31 having a cavity 37 (Fig. 16(B)).

(3) A plurality of chip capacitors 20 made of ceramic are accommodated onto the sheet 31c constituted by the uncured prepreg 33 (Fig. 16(C)).

10 (4) The top surfaces of the chip capacitors 20 are pushed or tapped to align the chip capacitors 20 into the same heights with each other (Fig. 16(D)). After that, a heat process is performed to cure the uncured prepreg 33 to form a substrate 31. The subsequent processes are the same as those of the first modification which has been described above with reference to Figs. 9 to 15, and therefore, their description will be omitted. (Third Modification of First Embodiment)

15 20 A structure of a printed circuit board according to a third modification of the first embodiment will be described referring to Fig. 18.

The printed circuit board according to the third modification has the structure similar to that of the first embodiment, except for the structure of the chip capacitors 20 accommodated in the core substrate 30. Fig. 18 is a plan view showing the chip capacitors. Fig. 18(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 18(A), a chain line shows the cutting line. In the printed circuit board described in the first embodiment, as shown in the plan view of Fig. 18(B), the first electrodes 21 and the second electrodes 22 are

provide along the side ends of the chip capacitor. Fig. 18(C) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting according to the third modification. In Fig. 18(C), a chain line shows the cutting line. In the printed circuit board described in the third modification, as shown in the plan view of Fig. 18(D), the first electrodes 21 and the second electrodes 22 are provide inside the side ends of the chip capacitor.

In the printed circuit board according to the third modification, the chip capacitor 20 in which the electrodes are formed along an inside of the outer edge thereof is used. Therefore, a chip capacitor having a large capacity can be used as the chip capacitor 20.

A printed circuit board according to first alternative example of the third modification will be described referring to Fig. 19.

Fig. 19 is a diagram showing a plan view of the chip capacitor 20 to be accommodated in the core substrate of the printed circuit board according to a first alternative example. In the above-described first embodiment, a plurality of chip capacitors each having a small capacity are accommodated in the core substrate. Contrary to this, in the first alternative example, a large chip capacitor having a large capacity is accommodated in the core substrate. The chip capacitor 20 includes first electrodes 21, second electrodes 22, a dielectric body 23, a first conductive film 24 connected to the first electrodes 21, a second conductive film 25 connected to the second electrodes 22, and electrodes 27 which are not connected to the first conductive film 24 and the second conductive film 25 and used for connecting the upper and lower surfaces of the chip

capacitor. The chip capacitor is connected to the IC chip and the daughter board through the electrodes 27.

In the printed circuit board according to the first alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

Next, a printed circuit board according to a second alternative example will be described referring to Fig. 20. Fig. 20(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 20(A), a chain line shows the cutting line. Fig. 20 (B) is a diagram showing a plan view of the chip capacitor. In the second alternative example, as shown in Fig. 20(B), a plurality of chip capacitors from each of which a plurality of pieces are to be obtained by cutting (in Fig. 20(B), three pieces) are connected into one piece unit having a large size.

In the second alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

In the above-described embodiment, the chip capacitor is incorporated in the printed circuit board. Instead of the chip capacitor, it is also possible to use a plate-like capacitor in which a conductive film is formed on a ceramic plate.

(Fourth Modification of First Embodiment)

A printed circuit board according to a fourth modification of the first embodiment will be described with reference to Fig. 21. In the above-described first embodiment, the printed circuit board is provided with the chip capacitors 20 in the core substrate 30 alone. In the fourth modification, chip capacitors 120 having a large capacity are mounted on the surface of the printed circuit board.

The IC chip conducts a complicated calculation, and in the calculation processing, it instantaneously consumes a large electric power. In order to provide a large electric power to the IC chip, in this embodiment, chip capacitor 20 for power supply and chip capacitors 120 are provided to the printed circuit board. The effect of providing the chip capacitors 20 and 120 will be described with reference to Fig. 22.

In the graph of Fig. 22, a longitudinal axis indicates a voltage supplied to the IC chip, and a horizontal axis indicates a time. The chain double-dashed line C indicates the variation in the voltage supplied to the printed circuit board having no capacitor for power source. Without capacitor for power supply, the voltage is drastically attenuated. The broken line A indicates the variation in the voltage supplied to the printed circuit board having a chip capacitor on its surface. As compared with the case of the printed circuit board having no capacitor indicated by the chain double-dashed line C, the attenuation of voltage is not large. However, the length of loop becomes large, and sufficient electric power cannot be supplied in the rate determining step. That is, the voltage drastically drops down at the time of starting

the supply of electric power. The chain double-dashed line B, referring to Fig.8, indicates the voltage drop of the printed circuit board incorporating the chip capacitor. Whereas the length of the loop can be shortened, the voltage varies because a chip capacitor having a large capacitor cannot be accommodated on the core substrate 30. The solid line E indicates the variation in the voltage of the printed circuit board according to the fourth modification having chip capacitors 20 in its core substrate described above referring to Fig. 21, and the chip capacitors 120 having a large capacitor on its surface. The printed circuit board is provided with the chip capacitors 20 in the vicinity of the IC chip, and the chip capacitors 120 having a large capacity (and a relatively large inductance), thereby suppressing the variation in voltage to a minimum value.

As to the printed circuit board of the first embodiment, the inductance of the chip capacitors 20 embedded in the core substrate, and the inductance of the chip capacitors mounted on the back surface of the printed circuit board (on the surface at the side of daughter board) are shown as follows.

In the case of a single capacitor:

A capacitor of embedded type: 137pH

A capacitor of back surface mounted type: 287pH

In the case of eight capacitors connected in parallel:

Capacitors of embedded type: 60pH

Capacitors of back surface mounted type: 72pH

In both cases where a single capacitor is used and where a plurality of capacitors are connected in parallel to obtain an increased capacity, an inductance can be lowered by incorporating the chip capacitor.

Hereinafter, the results of reliability test will be described. In the test, the rate of change in the electrostatic capacity of a single chip capacitor in the printed circuit board of the first embodiment was measured.

Rate of change in electrostatic capacity
(measured at a frequency of 100Hz) (measured at a frequency of 1kHz)

Steam 168 hours:	0.3%	0.4%
HAST 100 hours:	-0.9%	-0.9%
TS 1000 cycles:	1.1%	1.3%

In the Steam test, the chip capacitor was subjected to steam to be kept at a moisture of 100%. In the HAST test, the chip capacitor was left for 100 hours at a relative moisture of 100%, an applied voltage of 1.3V, and at a temperature of 121°C. In the TS test, the chip capacitor was left for 30 minutes at -125°C, and 30 minutes for 55°C, and this test was repeated 1000 times.

In the above-described reliability test, it was realized that the printed circuit board incorporating the chip capacitors attains a reliability of the same level as the conventional printed capacitor on which a capacitor is mounted on its surface. As described above, in the TS test, even if an internal stress is generated due to the difference in the thermal expansion coefficients between the capacitor made of ceramic, and the core substrate 30 and the resin insulating layer 40 made of resin, no problems are created such as a disconnection between the first electrode 21, the second electrode 22 of the chip capacitor 20, and the via holes 60, a peeling of the chip capacitors 20 from the resin insulating layer 40, and the cracks in the resin

insulating layer 40. In this manner, high reliability can be attained over a long period of time.

In the first embodiment, as described above, a large cavity is formed and a plurality of capacitors are accommodated in the cavity. This structure makes it possible that the plurality of capacitors are reliably aligned at accurate positions on the core substrate with high density even if accuracy of the spot-facing process is low. In addition, the plurality of capacitors are placed in the cavity, the capacitors are aligned into the same heights with each other. Therefore, the insulating layer can be formed on the capacitors into a uniform thickness. The via holes and the conductor circuit can be properly formed, and the rate of generating defective printed circuit boards 10 can be lowered.

Since the resin is charged in the space between the core substrate and the capacitor, even if the stress is generated caused by the capacitors, the stress can be alleviated. In addition, no migration is created. As a result, neither peeling nor dissolution is caused between the electrodes of the capacitors and the connecting sections of the via holes. Due to these arrangements, the desired performance can be maintained in the reliability test. In the case where the capacitors are coated with copper, the generation of migration can be prevented.

(Second Embodiment)

First, the structure of a printed circuit board according to a second embodiment of the present invention will be described with reference to Figs. 29 and 30. Fig. 29 is a diagram showing a cross section of a printed circuit board 210. Fig. 30 is a diagram showing the state where an IC chip 290 is mounted on the printed circuit board

210 shown in Fig. 29, and the printed circuit board 210 is attached to a daughter board 294.

As shown in Fig. 29, the printed circuit board 210 incorporates chip capacitors 220, a core substrate 230 for accommodating chip capacitors 220, and an interlayer resin insulating layer 250 constituting the buildup layers 280A, 280B. The core substrate 230 is constituted by an accommodating layer 230a for accommodating the capacitors 220, and a connection layer 240. Via holes 260 and a conductor circuit 258 are formed in the connection layer 240. Via holes 360 and a conductor circuit 358 are formed in the interlayer resin insulating layer 250. In this embodiment, the buildup layer is constituted by a single interlayer resin insulating layer 250. As an alternative to this, the buildup layer may be constituted by a plurality of interlayer resin insulating layers.

As shown in Fig. 30, the via holes 360 in the upper buildup layer 280A are formed with bumps 276 to be respectively connected to pads 292S1, 292S2, 292P1, 292P2 of the IC chip 290. On the other hand, the via holes 360 in the lower buildup layer 280B are formed with bumps 276 to be respectively connected to pads 295S1, 295S2, 295P1, 295P2. Through holes 246 are formed in the core substrate 230.

As shown in Fig. 17(A), the chip capacitor 220 is constituted by a first electrode 221, a second electrode, 222, and an dielectric body 23 interposed between the first and second electrodes. The dielectric body 23 includes a plurality of first conductive films 24 connected to the first electrode 221 and a plurality of second conductive films 25 connected to the second electrode 222 in an opposed relation to each other. It

is preferable to cover the surfaces of the first electrode 221 and the second electrode 222 with an metallic coating such as copper plating. By coated with the metallic coating, the electric connection with the conductive adhesive 234 is improved, and the generation of migration can be prevented.

As shown in Fig. 30, The pad 292S2 for signal of the IC chip 290 is connected to the pad 295S2 for signal of the daughter board 294 through the bump 276-the conductor circuit 358-the via hole 360-the through hole 246-the via hole 360-the bump 276. On the other hand, the pad 292S1 for signal of the IC chip 290 is connected to the pad 295S1 for signal of the daughter board 294 through the bump 276-the via hole 360-the through hole 246-the via hole 360-the bump 276.

The pad 292P1 for power supply of the IC chip 290 is connected to the first electrode 221 of the chip capacitor 220 through the bump 276-the via hole 360-the conductor circuit 258-the via hole 260. On the other hand, the pad 295P1 for power supply of the daughter board 294 is connected to the first electrode 221 of the chip capacitor 220 through the bump 276-the via hole 360-the through hole 246-the conductor circuit 258-the via hole 260.

The pad 292P2 for power supply of the IC chip 290 is connected to the second electrode 222 of the chip capacitor 220 through the bump 276-the via hole 360-the conductor circuit 258-the via hole 260. On the other hand, the pad 295P2 for power supply of the daughter board 294 is connected to the second electrode 222 of the chip capacitor 220 through the bump 276-the via hole 360-the through hole 246-the conductor circuit 258-the via hole 260.

In the printed circuit board 210 of this embodiment, the chip capacitors 220 are placed immediately below the IC chip 290. The distance from the IC chip to each capacitor is shortened, and therefore, electric power can be instantaneously supplied to the IC chip. That is, the loop length which determines the loop inductance can be shortened.

In addition, the through hole 246 is formed between the chip capacitors 220, and no signal line passes through the chip capacitors 220. In this structure, there is no problem that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body.

The external substrate (i.e. daughter board) 294 to be connected to the back surface of the printed circuit board is connected to the first electrode 221 and the second electrode 222 of the capacitor 220 through the via hole 260 formed in the connection layer 240 on the side of IC chip and the through hole 246 formed in the core substrate 230. That is, although the accommodation layer 230a having a core material is hard to process, penetrating openings are formed in the accommodation layer 230a so that the terminal of the capacitor is not directly connected to the outside surface. As a result, the reliability of the connection can be increased.

As shown in Fig. 17(A), in this embodiment, a rough surface 23 α is formed on the surface of the dielectric body 23 made of ceramic of the chip capacitor 220. The rough surface 23 α contributes to an increased adhesion between the chip capacitor 220 made of ceramic and a resin insulating layer 240 made of resin, thereby avoiding the

resin insulating layer 240 from peeling from the interface with the chip capacitors 220 even when a heat cycle test is conducted. The rough surface 23a can be formed by polishing the surface of the chip capacitor 220 after the sintering step, or by roughening the surface of the chip capacitor 220 before the sintering step. In this embodiment, the surface of the chip capacitor is roughened to increase its adhesion with the resin insulating layer. Alternatively, the surface of the chip capacitor may be subjected to silane coupling process.

In this embodiment, a resin layer 236 is interposed between the side surface of the cavity 232 of the core substrate 230 and the chip capacitor 220. The thermal expansion coefficients of the resin layer 236 is set to the value lower than those of the core substrate 230 and the resin insulating layer 240, that is, are set to the value close to that of the chip capacitor 220 made of ceramics. In this manner, even if internal stress is generated between the core substrate 220 and the resin insulating layer 240, and the chip capacitor 20 caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur in the core substrate 230 and the connection layer 240. As a result, high reliability can be attained. In addition, the generation of migration can be prevented.

Next, the method for manufacturing the printed circuit board described above referring to Fig. 29 will be described with reference to Figs. 23 to 28.

(1) A connection layer, which is a resin layer constituting the core substrate, is formed. On one surface of the connection layer, a circuit pattern

constituted by a metallic layer is formed. For this purpose, a resin film 240a having a metal film 257 laminated on its one surface is prepared (Fig. 23(A)). The resin film 240a may be made of, as is the case of the first embodiment, thermosetting resin such as epoxy, BT, polyimide, and olefin, or mixtures of thermosetting resins and thermoplastic resins. In this embodiment, it is preferable to use a film having no core material so that the penetrating openings can be easily formed. The metal film 257 is pattern-etched to form a predetermined circuit pattern 257 α (Fig. 23(B)). The chip capacitors 220 are attached to the circuit pattern 257 α located on the lower surface of the resin film 240a through the conductive adhesive material 234c (Fig. 23(C)). In this manner, the electrical connection with the capacitors 220 and the adhesion between the capacitors 220 and the circuit pattern 257 α can be assured. The conductive adhesive material 234 may be a material having both conductivity and adhesiveness such as a solder (Sn/Pb, Sn/Sb, Sn/Ag, Sn/Ag/Cu), conductive pastes, and resins impregnated with metal particles. The space created between the conductive adhesive and the capacitor is preferably filled with a resin.

(2) On the other hand, a laminated plate 232a for accommodation layer formed with cavities 232 for accommodating chip capacitors is prepared (Fig. 23(C)).

The cavities 232 are formed by spot-facing process. Instead of spot-facing process, the cavities may be formed in the laminated late by bonding a prepreg formed with penetrating openings and a prepreg formed with no penetrating openings, or by injection molding. The laminated plate 232a for accommodation layer may be a

laminated plate formed by laminating prepregs each having a core member such as glass cloth impregnated with an epoxy resin. Instead of the laminated plate having a core member impregnated with epoxy resin, it is also possible to use a laminated plate generally used in a printed circuit board, such as those having a core member impregnated with BT, phenolic resins, or a reinforcement member such as glass cloth. It is also possible to use a resin substrate having no core member such as glass cloth. However, it is impossible to use a substrate of ceramic or AlN as the core substrate. The substrate of ceramic or AlN is poor in processability for outer shape, and in some cases, is incapable of accommodating capacitors. In addition, a space is created inside the substrate even if it is filled with a resin. Since a resin substrate has a melting point of 300°C or lower, it is dissolved or softened when a heat higher than 350°C is applied.

(3) The resin film 240a to which the chip capacitors 220 are attached, a resin laminated plate 232a for core substrate having sections for accommodating capacitors, and another resin film 240a are laminated to each other, and are pressed from both sides to flatten the surface (Fig. 23(D)). In this embodiment, the accommodation layer 230a which accommodates the capacitors 220 and the connection layer 240 are bonded to each other by application of pressure from both sides to form a core substrate 230. As a result, the core substrate 230 has a flat surface. The interlayer resin insulating layer 250 and the conductor circuit 358 can be laminated in a later step in such a manner that high reliability is attained. At this time, the space between

the capacitor 220 and the resin film 240a is filled with a resin exuding from the resin film 240a. If the space cannot sufficiently filled with the resin, as shown in Fig. 24(A), a small-sized filler 236a having a thermal expansion coefficient smaller than that of the core substrate is provided between the circuit patterns 257 α on the side of the resin film 240a, so that the space is filled with the filler 236a as shown in Fig. 24(D). Alternatively, as shown in Fig. 24(C), the filler 236a may be placed on the capacitor 220, so that the space is filled with the filler 236a as shown in Fig. 24(D).

(4) Heating and curing is conducted to form a core substrate 230 constituted by an accommodation layer 230a accommodating the chip capacitors 220 and a connection layer (Fig. 25(A)). It is preferable that a resin layer 236 having a thermal expansion coefficient smaller than that of the core substrate is charged in the cavity 232 of the core substrate to increase the air tightness. In this embodiment, a resin film 240a having no metal layer is laminated. As an alternative to this, a resin film (RCC) having a metal layer on its one side may be used. That is, it is possible to use a both-sided plate, a one-sided plate, a resin plate having no metal film, and a resin film.

(5) In this embodiment, a circuit pattern 257 α to be connected to the conductive adhesive 234 is provided between the connection layer 240 and the accommodating layer 230 which form the core substrate 230 together. With this arrangement, the connection to the capacitors 220 is reliably established through the circuit pattern 257 α . In addition, since circuit pattern 257 α is provided between the connection layer

240 and the accommodation layer 230a, the warpage of the core substrate 230 can be prevented.

(6) Non-penetrating openings 248 to be via holes are formed in the upper connection layer 240 by CO₂ laser, YAG laser, excimer laser, or UV laser (Fig. 25(B)). As the case may be, an area mask on which penetrating openings are formed at positions corresponding to the positions of the non-penetrating openings are mounted, and an area processing is conducted by a laser. In the case where it is desired to form via holes having different sizes and diameter from each other, the lasers may be used in combination to form the via holes.

(7) If necessary, smear in the via holes may be conducted by a gas plasma treatment using gaseous matter such as oxygen and nitrogen, or dry treatment such as corona treatment, or by immersion into an oxidizer such as permagnetic acid. Subsequently, penetrating openings 246a having a diameter of 50 to 500 μ m for through holes are penetrated in the core substrate 230 constituted by the connection layer 240, the accommodation layer 230a, and the connection layer 240 by a drill or a laser (Fig. 25(C)).

(8) A metal film is formed on the surface layer of the connection layer 240, the non-penetrating openings 248 for via holes, and the penetrating openings 246a for through holes of the core substrate 230. For this purpose, a palladium catalyst is provide on the surface of the connection layer 240, and then, the core substrate 230 is immersed in an electroless plating solution to uniformly precipitate an electroless copper plated film 252 (Fig. 26(A)). In this embodiment, an electroless plating is employed. Alternatively, a metal film of

copper, nickel and the like may be formed by sputtering. The sputtering is disadvantageous from the viewpoint of cost, but is advantageous in that the adhesion with the resin film can be improved. An electroless plated film may be formed after the metal layer is formed by sputtering. Depending on the kind of resin, there are cases where the catalyst cannot be stably provided thereto. In this case, the electroless plated film is effective in stably providing the catalyst to such a resin. In addition, the electrolytic plating is more stably precipitated in the case of forming the electroless plated film. The metal film 252 is preferably formed into the thickness of 0.1 to 3mm.

(9) A photosensitive dry film is attached to the surface of the metal film 252, and a mask is placed thereon. Exposure to light and development are performed to form a resist 254 having a predetermined pattern. The core substrate 230 is immersed into an electrolytic plating solution to allow a current to flow in the core substrate 230 through the electroless plated film 252 to precipitate an electrolytic copper plated film 252 (Fig. 26(B)). The resist 254 is peeled by 5% KOH, and then, the electroless plated film 252 located under the resist 254 is etched and removed by a mixed solution of sulfuric acid and hydrogen peroxide. As a result, via holes 260 and a conductor circuit 258 are formed in the connection layer 240, and through holes 246 are formed in the penetrating openings 246a of the core substrate 230 (Fig. 26(C)).

(10) A rough surface is formed on the surface of the conductive layer of the conductor circuit 258, the via holes 260, and the through holes 246. The rough surface is formed by oxidizing (i.e. blacking)-reduction

treatment, an electroless plated film made of alloys of Cu-Ni-P, or by etching treatment using an etching solution containing cupric complex and an organic acid. The rough surface has Ra (mean roughness height) of 0.01 to 5 μ m, and especially preferable is Ra of 0.5 to 3 μ m. In this embodiment, the rough surface is formed. Alternatively, as will be described later, a resin is directly filled and a resin film may be attached.

(11) The through holes 246 are filled with a resin layer 262. The resin layer may be made of a resin having no conductivity and containing a epoxy resin as a main component, or a resin having conductivity and containing a paste of metal such as copper. In this case, the thermosetting epoxy resin containing a silica for adjusting the thermal expansion coefficient is charged as a resin filler. After the through holes 246 are filled with the resin layer 262, the resin film 250 is attached (Fig. 27(A)). Instead of attaching the resin film 250, a resin may be applied. After the resin film 250 is attached, via holes 348 having an opening diameter of 20 to 250 μ m are formed in the insulating layer 250, and thermosetting is conducted (Fig. 27(B)). Then, a catalyst is provided to the core substrate, and the core substrate is immersed in electroless plating to uniformly precipitate an electroless plated film 352 having a thickness of 0.9 μ m on the surface of the interlayer resin insulating layer 250. After that, a resist 354 having a predetermined pattern is formed (Fig. 27(C)).

(12) The core substrate is immersed in an electrolytic plating solution to allow a current to flow in the core substrate through the electroless plated film 352 to form an electrolytic copper plated film 356 in

the portions where no resist 354 is formed (Fig. 28(A)). The resist 354 is peeled and removed, and then, the electroless plated film 352 located under the plated resist is dissolved and removed to obtain a conductor circuit 358 constituted by the electroless plated film 352 and the electrolytic copper plated film 356 and via holes 360 (Fig. 28(B)).

(13) A rough surface (not shown) is formed on the surface of the conductor circuit 358 and the via holes 360 by an etching solution containing cupric complex and an organic acid. It is also possible to further performing Sn substitution on the rough surface.

(14) Solder bumps are formed on the above-described printed circuit board. On both sides of the substrate, a solder resist composition is applied, and drying is performed. After that, a photomask film (not shown) on which a circular pattern (i.e. mask pattern) is drawn is made hermetic contact and placed onto the solder resist composition, and is exposed to UV ray and then is developed. Furthermore, heating is performed to form a solder resist layer (having a thickness of $20\mu\text{m}$) having openings 271U, 271D at solder pad portions (including via holes and land portions thereof) (Fig. 28(C)).

(15) The openings 271U, 271D of the solder resist layer 270 are filled with a solder paste (not shown). Then, the solder charged into the openings 271U, 271D is reflowed at 200°C to form solder bumps (i.e. solder bodies) 276 are formed (Fig. 29). In order to increase the corrosion resistance, a layer of metal such as Ni, Au, Ag, Pd and the like may be formed in the opening 271 by plating or sputtering.

The processes of mounting the IC chip on the printed circuit board, and attaching the printed circuit board to the daughter board are the same as those of the first embodiment, and their description will be omitted.

5 (First Modification of Second Embodiment)

A printed circuit board according to a first modification of the second embodiment will be described with reference to Fig. 31. The printed circuit board according to a first modification has a similar structure
10 as of second modification, except for the following points. That is, in the printed circuit board of the first modification, conductive pints 296 are provided, and a connection with the daughter board is established through the conductive pins 296. Whereas the resin film
15 240a having the metal film 257 on its one side is employed in the foregoing embodiment described above referring to Fig. 23(A), in the first modification, a resin film having metal films on its both sides is employed to manufacture an interlayer resin insulating layer 240 on
20 the side of IC chip 290. That is, the upper metal film is pattern-etched to form a circuit pattern 257 α . Furthermore, non-penetrating openings 248 are formed by a laser to form via holes 260 using openings 257a of the circuit pattern 257 α as conformal masks.

25 Whereas in the second embodiment described above, chip capacitors 220 are accommodated in the core substrate 230 alone, in the first modification, chip capacitors 320 each having a large capacity are mounted on the front surface and back surface of the core substrate
30 230, on top of the chip capacitors 220 accommodated in the core substrate 230.

The IC chip conducts a complicated calculation,

and in the calculation processing, it instantaneously consumes a large electric power. In order to provide a large electric power to the IC chip, in this modification, chip capacitors 420 for power supply and chip capacitors 520 are provided to the printed circuit board. The effect of providing the chip capacitors 420 and 520 is the same as that attained in the fourth modification of the first embodiment, and therefore, its description will be omitted.

(Second Modification of Second Embodiment)

A printed circuit board according to a second modification of the second embodiment will be described with reference to Fig. 32. The printed circuit board according to the second modification has the similar structure as of the second embodiment described above, except for the following points. That is, in the printed circuit board according to the second modification, the first electrode 221 and the second electrode 222 of the chip capacitor 220 are directly connected to each other through pads 292P1, 292P2 for power supply of the IC chip 290, and a bump 276. In the second modification, the distance between the IC chip and each chip capacitor can be further shortened.

(Third Modification of Second Embodiment)

A printed circuit board according to a third modification of the second embodiment will be described with reference to Fig. 33. The printed circuit board according to the third modification has the similar structure as of the second embodiment, except for the following points. That is, in the printed circuit board according to the third modification, the first electrode 221, the second electrode 222 of the capacitor 220 are directly connected to the through hole 246 by a circuit

pattern 257 α provided between the accommodation layer 230a and the connection layer 240. In the third modification, the wire length from the first electrode 221 and the second electrode 222 to the daughter board can be shortened.

(Fourth Modification of Second Embodiment)

A printed circuit board according to a fourth modification of the second embodiment will be described with reference to Fig. 18.

The printed circuit board according to the fourth modification has the similar structure as of the first modification described above, except for the chip capacitors 20 accommodated in the core substrate 30. Fig. 18 is a plan view showing the chip capacitor. Fig. 18(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 18(A), a chain line shows the cutting line. In the printed circuit board described in the first embodiment, as shown in the plan view of Fig. 18(B), the first electrodes 21 and the second electrodes 22 are provide along the side ends of the chip capacitor. Fig. 18(C) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting according to the fourth modification. In Fig. 18(C), a chain line shows the cutting line. In the printed circuit board described in the fourth modification, as shown in the plan view of Fig. 18(D), the first electrodes 21 and the second electrodes 22 are provided inside the side ends of the chip capacitor.

In printed circuit board of the fourth modification, the chip capacitor 20 in which the electrodes are formed along an inside of the outer edge

thereof is used. Therefore, a chip capacitor having a large capacity can be used as the chip capacitor 20.

A printed circuit board according to first alternative example of the fourth modification will be described referring to Fig. 19.

Fig. 19 is a diagram showing a plan view of the chip capacitor 20 to be accommodated in the core substrate of the printed circuit board according to a first alternative example. In the above-described first embodiment, a plurality of chip capacitors each having a small capacity are accommodated in the core substrate. Contrary to this, in the first alternative example, a large chip capacitor 20 having a large capacity is accommodated in the core substrate. The chip capacitor 20 includes first electrodes 21, second electrodes 22, a dielectric body 23, a first conductive film 24 connected to the first electrodes 21, a second conductive film 25 connected to the second electrodes 22, and electrodes 27 which are not connected to the first conductive film 24 and the second conductive film 25 and used for connecting the upper and lower surfaces of the chip capacitor. The chip capacitor is connected to the IC chip and the daughter board through the electrodes 27.

In the printed circuit board according to the first alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

Next, a printed circuit board according to a second alternative example will be described referring to Fig.

20. Fig. 20(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 20(A), a chain line shows the cutting line. Fig. 20 (B) is a diagram showing a plan view of the chip capacitor. In the second alternative example, as shown in Fig. 20(B), a plurality of chip capacitors from each of which a plurality of pieces are to be obtained by cutting (in Fig. 20(B), three pieces) are connected into one piece unit having a large size.

In the second alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

In the above-described embodiment, the chip capacitors are incorporated in the printed circuit board. Instead of the chip capacitor, it is also possible to use a plate-like capacitor in which a conductive film is formed on a ceramic plate.

As to the printed circuit board of the second embodiment, the inductance of the chip capacitor 220 embedded in the core substrate, and the inductance of the chip capacitor mounted on the back surface of the printed circuit board (on the surface at the side of daughter board) are shown as follows.

In the case of a single capacitor:

A capacitor of embedded type: 137pH

A capacitor of back surface mounted type: 287pH

In the case of eight capacitors connected in parallel:

Capacitors of embedded type: 60pH

Capacitors of back surface mounted type: 72pH

In both cases where a single capacitor is used and where a plurality of capacitors are connected in parallel to obtain an increased capacity, an inductance can be lowered by incorporating the chip capacitor.

5 Hereinafter, the results of reliability test will be described. In the test, the rate of change in the electrostatic capacity of a single chip capacitor in the printed circuit board of the second embodiment was measured.

10 Rate of change in electrostatic capacity
(measured at a frequency of 100Hz) (measured at a
frequency of 1kHz)

Steam 168 hours: 0.3% 0.4%

HAST 100 hours: -0.9% -0.9%

15 TS 1000 cycles: 1.1% 1.3%

In the Steam test, the chip capacitor was subjected to steam to be kept at a moisture of 100%. In the HAST test, the chip capacitor was left for 100 hours at a relative moisture of 100%, an applied voltage of 1.3V,
20 and at a temperature of 121°C. In the TS test, the chip capacitor was tested for 30 minutes at -125°C, and 30 minutes for 55°C, and this test was repeated 1000 times.

In the above-described reliability test, it was realized that the printed circuit board incorporating
25 the chip capacitor attains a reliability of the same level as the conventional printed capacitor on which a capacitor is mounted on its surface. As described above, in the TS test, even if an internal stress is generated due to the difference in the thermal expansion
30 coefficients between the capacitor 220 made of ceramic, and the core substrate 230 and the connection layer 240 made of resin, no problems are created such as a peeling

of the chip capacitor 220 from the connection layer 240, and the cracks in the core substrate 230 and the connection layer 240. In this manner, high reliability can be attained over a long period of time.

5 According to the structure of the second embodiment, there is no problem of lowering the electric characteristics caused by inductance.

10 Since the resin is charged in the space between the core substrate and the capacitor, even if the stress is generated caused by the capacitors, the stress can be alleviated. In addition, no migration is created. As a result, neither peeling nor dissolution is caused between the electrodes of the capacitor and the connecting sections of the via holes. Due to these
15 arrangements, the desired performance can be maintained in the reliability test.

 In the case where the capacitors are coated with copper, the generation of migration can be prevented.
(Third Embodiment)

20 First, the structure of a printed circuit board according to a third embodiment of the present invention will be described with reference to Figs. 37 and 38. Fig. 37 is a diagram showing a cross section of a printed circuit board 410. Fig. 38 is a diagram showing the state where
25 an IC chip 490 is mounted on the printed circuit board 410 shown in Fig. 37, and the printed circuit board 410 is attached to a daughter board 494.

 As shown in Fig. 37, the printed circuit board 410 incorporates chip capacitors 420, a core substrate
30 430 for accommodating chip capacitors 420, and an interlayer resin insulating layer 450 constituting the buildup layers 480A, 480B. The core substrate 430 is constituted by an accommodating layer 430a for

accommodating the capacitors 420, and a connection layer 440. Via holes 460 and a conductor circuit 458 are formed in the connection layer 440. Via holes 560 and a conductor circuit 558 are formed in the interlayer resin insulating layer 450. In this embodiment, the buildup layer is constituted by a single interlayer resin insulating layer 450. As an alternative to this, the buildup layer may be constituted by a plurality of interlayer resin insulating layers.

As shown in Fig. 45, the chip capacitor 420 is constituted by a first electrode 421, a second electrode 422, and a dielectric body 423 interposed between the first and second electrodes. The dielectric body 423 includes a plurality of first conductive film 424 connected to the first electrode 421 and a plurality of second conductive film 425 connected to the second electrode 422 in an opposed relation to each other. In this embodiment, a connection for the first electrode 421 and the second electrode 422 is established by forming via holes 460 made of plating. As shown in Fig. 45, a metal (i.e. copper) layer 426 is exposed from the upper coating layer 428 formed on the first electrode 421 and the second electrode 422. With this arrangement, as shown in Fig. 37, the connection with the via holes 460 made of copper plating is enhanced, and the connection resistance can be lowered.

As shown in Fig. 38, the via holes 560 in the upper buildup layer 480A are formed with bumps 476 to be respectively connected to pads 492S1, 492S2, 492P1, 492P2 of the IC chip 490. On the other hand, the via holes 560 in the lower buildup layer 480B are formed with bump 476 to be respectively connected to pads 495S1, 495S2, 495P1, 495P2. Through holes 446 are formed in the core

substrate 430.

The pad 492S2 for signal of the IC chip 490 is connected to the pad 495S2 for signal of the daughter board 494 through the bump 476-the conductor circuit 558-the via hole 560-the through hole 446-the via hole 560-the bump 476. On the other hand, the pad 492S1 for signal of the IC chip 490 is connected to the pad 495S1 for signal of the daughter board 494 through the bump 476-the via hole 560-the through hole 446-the via hole 560-the bump 476.

The pad 492P1 for power supply of the IC chip 490 is connected to the first electrode 421 of the chip capacitor 420 through the bump 476-via hole 560-the conductor circuit 458-the via hole 460. On the other hand, the pad 495P1 for power supply of the daughter board 494 is connected to the first electrode 421 of the chip capacitor 420 through the bump 476-the via hole 560-the through hole 446-the conductor circuit 458-the via hole 460.

The pad 492P2 for power supply of the IC chip 490 is connected to the second electrode 422 of the chip capacitor 420 through the bump 476-the via hole 560-the conductor circuit 458-the via hole 460. On the other hand, the pad 495P2 for power supply of the daughter board 494 is connected to the second electrode 422 of the chip capacitor 420 through the bump 476-the via hole 560-the through hole 446-the conductor circuit 458-the via hole 460.

In the printed circuit board 410 of the third embodiment, the chip capacitors 420 are placed immediately below the IC chip 490. The distance from the IC chip to each capacitor is shortened, and therefore, electric power can be instantaneously supplied to the

IC chip. That is, the loop length which determines the loop inductance can be shortened.

In addition, the through hole 446 is formed between the chip capacitors 420, and no signal line passes through the chip capacitors 420. In this structure, there is no problem that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body.

The external substrate (i.e. daughter board) 494 to be connected to the back surface of the printed circuit board is connected to the first electrode 421 and the second electrode 422 of the capacitor 420 through the via holes 460 formed in the connection layer 440 on the side of IC chip and the through holes 446 formed in the core substrate 430. That is, although the accommodation layer 430a having a core material is hard to process, penetrating openings are formed in the accommodation layer 430a so that the terminal of the capacitor is not directly connected to the external substrate. As a result, the reliability of the connection can be increased.

In this embodiment, as shown in Fig. 37, an adhesive 436 is interposed between the lower surface of the penetrating opening 437 of the core substrate 430 and the chip capacitor 420. In addition, a resin filling agent 436a is charged in a space between the side surface of the penetrating opening 437 and the chip capacitor 420. The thermal expansion coefficients of the resin layer 436 and the adhesive material 436a provided on the bottom surface of the chip capacitor 420 are set to the values lower than those of the core substrate 430 and the connection layer 440, that is, are set to the values

close to that of the chip capacitor 420 made of ceramics. In this manner, even if internal stress is generated between the core substrate 430 and the connection layer 440, and the chip capacitor 420 caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur in the core substrate and the connection layer 440. As a result, high reliability can be attained. In addition, the generation of migration can be prevented.

The process of manufacturing the printed circuit board of the third embodiment will be described with reference to Figs. 34 to 37.

(1) Four prepregs 435 each having a core material impregnated with an epoxy resin are laminated on top of each other to form a laminated plate 432a, and penetrating openings 437 for accommodating chip capacitors are formed in the laminated plate 432a. On the other hand, two prepregs 435 are laminated on top of each other to form a laminated plate 432b (Fig. 34(A)). Instead of the epoxy resin, the prepreg 435 may be impregnated with BT, phenolic resin, or reinforcement material such as glass cloth. The laminated plate 432a and the laminated plate 432b are laminated to each other to form an accommodation layer 430a. Then, as described above referring to Fig. 45(A), chip capacitors 420 in which a coating layer 428 is peeled from the first and second electrodes 421, 422 are accommodated in the penetrating opening 437 (Fig. 34(B)). It is preferable that an adhesive 436 is interposed between the penetrating opening 437 and the chip capacitor 420. The resin and interlayer resin insulating layer used in this invention has melting points of 300°C or lower. Therefore, when heat higher

than 350°C is applied, the resin and interlayer resin insulating layer may be dissolved, softened, or carbonized. As the adhesive 436, it is preferable to use an adhesive having a thermal expansion coefficient smaller than that of the core substrate.

It is impossible to use substrates made of ceramic and AlN as the core substrate. These substrates are poor in outer shape processing characteristics, and cannot accommodate capacitors in some cases, because a space is created inside the substrate even if it is filled with a resin.

(2) The resin film 440a (i.e. a connection layer) is laminated on both sides of the accommodating layer constituted by the laminated plate 432a and the laminated plate 432b and accommodating the chip capacitors 420 (Fig. 34(C)), and are pressed from both sides to flatten the surface. Then, the resultant is heated and cured to form a core substrate 430 constituted by the accommodating layer 430a accommodating the chip capacitors 420 and the connection layer 440 (Fig. 34(D)). In this embodiment, the accommodation layer 430a which accommodates the capacitors 420 and the connection layer 440 are bonded to each other by application of pressure from both sides to form the core substrate 430. As a result, the core substrate 430 has a flat surface. The interlayer resin insulating layer 450 and the conductor circuit 458 can be laminated in a later step in such a manner that high reliability is attained.

It is preferable that a resin filler 436a is charged in the side surface of the penetrating openings 437 of the core substrate to increase the air tightness. As the resin filler 436a, it is preferable to use a filler

having a thermal expansion coefficient smaller than that of the core substrate. In this embodiment, the resin film 440a may be a resin film of the same type as that used in the first embodiment which has no metal layer.

5 As an alternative to this, a resin film (RCC) having a metal layer on its one side may be used. That is, it is possible to use a both-sided plate, a one-sided plate, a resin plate having no metal film, and a resin film.

(3) Penetrating openings 446 each having a
10 diameter of 300 to 500 μ m for through holes are formed in the core substrate and the interlayer resin insulating layer 450 with a drill (Fig. 35(A)). Non-penetrating openings 448 extending to the first electrode 421 and the second electrode 422 of the chip capacitor 420 are
15 formed in the upper interlayer resin insulating layer 450 by CO₂ laser, YAG laser, excimer laser, or UV laser (Fig. 35(B)). As the case may be, an area mask on which penetrating openings are formed at positions
corresponding to the positions of the non-penetrating
20 openings is mounted, and an area processing is conducted by a laser. In the case where it is desired to form via holes having different sizes and diameter from each other, the lasers may be used in combination to form the via
holes.

25 (4) A desmear process is performed. Subsequently, a palladium catalyst is provided to the surface of the substrate 430, and then, the core substrate 430 is immersed into an electroless plating solution to uniformly precipitate the electroless plated film 452
30 (Fig. 35(C)). As a result of this, a rough layer can be formed on the surface of the electroless copper plated film 452. The rough surface has Ra (mean roughness

height) of 0.01 to 5 μ m, and especially preferable is Ra of 0.5 to 3 μ m.

(6) A photosensitive dry film is attached on the surface of the electroless plated film 452, and a mask is mounted thereon. Exposure to light and development are performed to form a resist 454 having a predetermined pattern (Fig. 36(A)). In this embodiment, an electroless plating is employed. Alternatively, a metal film of copper, nickel and the like may be formed by sputtering. The sputtering is disadvantageous from the viewpoint of cost, but is advantageous in that the adhesion with the resin can be improved. The core substrate 430 is immersed in an electrolytic plating solution, and a current is allowed to flow in the core substrate 430 through the electroless plated film 452 to precipitate an electrolytic copper plated film 456 (Fig. 36(B)). The resist 454 is peeled by 5% KOH, and the electroless plated film 452 located under the resist 454 is etched and removed with a mixed solution of sulfuric acid and hydrogen peroxide. As a result, via holes 460 are formed in the non-penetrating openings 448 of the connection layer 440, a conductor circuit 458 is formed on the surface of the connection layer 440, and through holes 446 are formed in the penetrating openings 446a of the core substrate 430 (Fig. 36(C)). The subsequent processes are the same as the steps (10) to (15) of the second embodiment which has been described above, and therefore, their description will be omitted.

The processes of mounting the IC chip on the printed circuit board, and attaching the printed circuit board to the daughter board are the same as those of the first embodiment, and their description will be omitted.

(First Modification of Third Embodiment)

A printed circuit board according to a first modification of the third embodiment will be described with reference to Fig. 39. The printed circuit board according to the first modification has the similar structure as of the first modification described above, except for the following points. That is, in the printed circuit board of the first modification, conductive pins 496 are provided, and a connection with the daughter board is established through the conductive pins 496.

Whereas in the third embodiment described above, chip capacitors 420 are accommodated in the core substrate 430 alone, in the first modification, chip capacitors 520 each having a large capacity are mounted on the front surface and back surface of the core substrate 430, on top of the chip capacitors 420 accommodated in the core substrate 430.

The IC chip conducts a complicated calculation, and in the calculation processing, it instantaneously consumes a large electric power. In order to provide a large electric power to the IC chip, in the first modification, chip capacitors 420 for power supply and chip capacitors 520 are provided to the printed circuit board. The effect of providing the chip capacitors 420 and 520 is the same as that attained in the fourth modification of the first embodiment, and therefore, its description will be omitted.

(Second modification of Third Embodiment)

A printed circuit board according to a second modification of the third embodiment will be described with reference to Fig. 42. The printed circuit board according to the second modification has the similar structure as of the third modification described above,

except for the following points. In the third embodiment, the core substrate 430 is constituted by the accommodation layer 430a having connection layers 440 on its both sides. Contrary to this, in the second
5 embodiment, the connection layer 440 is formed only on the upper surface of the accommodation layer 430a.

The processes of manufacturing the printed circuit board according to the second modification of the third embodiment will be described with reference
10 to Figs. 39 to 41.

(1) Four prepregs 435 impregnated with an epoxy resin are laminated on top of each other to form a laminated plate 432a, and penetrating openings 437 for
15 accommodating chip capacitors are formed in the laminated plate 432a. On the other hand, two prepregs 435 are laminated on top of each other to form a laminated plate 432b (Fig. 40(A)). Chip capacitors 420 are mounted through the adhesives 436 on the laminated plate 432b at positions corresponding to the penetrating openings
20 of the laminated plate 432a (Fig. 40(B)). The laminated plate 432a and the laminated plate 432b are laminated to each other to form an accommodating layer 430a accommodating the chip capacitors 420 (Fig. 40(C)).

(2) The resin film 440a (i.e. a connection layer)
25 is laminated on the accommodating layer constituted by the laminated plate 432a and the laminated plate 432b, and accommodating the chip capacitors 420 (Fig. 40(D)), and the resultant is pressed from both sides to flatten the surface. Then, heating and curing is conducted to
30 form a core substrate 430 constituted by the accommodating layer 430a accommodating the chip capacitors 420 and the connection layer 440 (Fig. 41(A)). In this embodiment, the accommodation layer 430a which

accommodates the capacitors 420 and the connection layer 440 are bonded to each other by application of pressure from both sides to form the core substrate 430. As a result, the core substrate 430 has a flat surface. The interlayer resin insulating layer 450 and the conductor circuit 558 can be laminated in such a manner that high reliability is attained.

(3) Penetrating openings 446 each having a diameter of 300 to 500 μ m for through holes are formed in the core substrate and the interlayer resin insulating layer 450 with a drill (Fig. 41(B)). Non-penetrating openings 448 extending to the first electrode 421 and the second electrode 422 are formed in the upper interlayer resin insulating layer 450 by CO₂ laser, YAG laser, excimer laser, or UV laser (Fig. 41(C)). The subsequent processes are the same as the steps (3) and after of the third embodiment, and therefore, their description will be omitted.

(Third Modification of Third Embodiment)

A printed circuit board according to third modification of the third embodiment will be described with reference to Fig. 44. The printed circuit board according to the third modification has the similar structure as of the second modification of the third embodiment described above, except for the following points. That is, in the printed circuit board according to the second modification, via holes 460 are formed on only one surface of the core substrate 430 on the IC chip side. Contrary to this, in the third modification, via holes 460 are formed on both surfaces of the core substrate on the sides of IC chip and daughter board.

In the third modification, the via holes 460 are

formed not only on the front surface but also on the back surface. In this manner, the wire length between the chip capacitors 420 and the daughter board can be shortened.

5 The processes of manufacturing the printed circuit board according to the third modification of the third embodiment will be described with reference to Fig. 43.

10 (1) Four prepregs 435 impregnated with an epoxy resin are laminated on top of each other to form a laminated plate 432a, and penetrating openings 437 for accommodating chip capacitors are formed in the laminated plate 432a. On the other hand, two prepregs 435 are laminated on top of each other to form a laminated plate 15 432b, and penetrating openings 439 extending to the electrodes are formed at positions where the chip capacitors are to be mounted (Fig. 43(A)). Chip capacitors 420 are mounted on the laminated plate 432b through the adhesive material 436 at positions 20 corresponding to the penetrating openings formed in the laminated plate 432a (Fig. 43(B)). The laminated plate 432a and the laminated plate 432b are laminated to each other to form an accommodating layer 430a (Fig. 43(C)).

25 (2) The resin film 440a (i.e. a connection layer) is laminated on the upper surface of the accommodating layer 430a (Fig. 43(D)), and are pressed from both sides to flatten the surface. Then, the resultant is heated and cured to form a core substrate 430 constituted by the accommodating layer 430a accommodating the chip 30 capacitors 420 and the connection layer 440 (Fig. 44). The subsequent processes are the same as the steps (3) and after of the third embodiment, and therefore, their description will be omitted.

(Fourth Modification of Third Embodiment)

A printed circuit according to fourth modification of the third embodiment will be described referring to Figs. 46 and 47.

5 The printed circuit board according to the fourth modification has the similar structure as of the third embodiment described above referring to Fig. 37, except for the following points. That is, in the printed circuit board according to the fourth modification, as
10 shown in Fig. 47, in the chip capacitor 420, the coating layer 428 (Fig. 45(A)) is completely peeled from the first and second electrodes 421, 422, and then, the first and second electrodes are coated with a copper plated film 429. An electric connection for the first and second
15 electrodes 421, 422 coated with the copper plated film 429 is established through via holes 460 constituted by a copper plating. The electrodes 421, 422 of the chip capacitor are metallized and has pits and projections on their surfaces. If the metal layer 426 is left
20 uncoated and exposed to the outside, the resin may be left in the pits and projections in the step of forming non-penetrating openings 448 in the connection layer 440. The resin left in the pits and projections may cause a disconnection between the first and second electrodes
25 421, 422 and the via hole 460. Contrary to this, in the fourth modification, the surfaces of the first and second electrodes 421, 422 coated with the copper plated film 429 are flat and smooth. When the non-penetrating openings 448 are formed in the connection layer 440 formed
30 on the electrodes, no resin is left on the surfaces of the electrodes. When the via holes 460 are formed, the connection between the via holes 460 and the electrodes 421, 422 has increased reliability.

Since the via holes 460 are made by plating into the electrodes 421, 422 formed with the copper plated film 429, the electrodes 421, 422 are firmly connected to the via holes 460. No disconnection occurs between the electrodes 421, 422 and via holes 460 even when a heat cycle test is conducted. No migration is generated, and in addition, no problem arises at the connection in the via holes of the capacitor.

The copper plated film 429 is formed after a nickel/tin layer (i.e. coating layer) provided onto the surface of the metal layer 426 in the step of manufacturing the chip capacitor is peeled off at the time of mounting the chip capacitor onto the printed circuit board. Alternatively, the copper plated film 429 may be directly provided onto the surface of the metal layer 426 in the step of manufacturing the chip capacitor 420. In the fourth modification, as is the case of the third embodiment, openings which extend to the copper plated film 429 of the electrodes are formed by a laser, and then a desmear process is performed to form via holes by copper plating. Therefore, even if an oxide film is formed on the surface of the copper plated film 429, the oxide film can be removed in the laser or desmear process.

On the surface of the dielectric body 423 made of ceramic of the chip capacitor 420, a rough surface 423 α is formed. The rough surface 423 α contributes to an increased adhesion between the chip capacitor 420 made of ceramic and the connection layer 440 made of resin, thereby avoiding the connection layer 440 from peeling from the interface with the chip capacitor 420 even when a heat cycle test is conducted. The rough surface 423 α can be formed by polishing the surface of the chip

capacitor 420 after the sintering step, or by roughening the surface of the chip capacitor 420 before the sintering step. In the fourth modification, the surface of the chip capacitor is roughened to increase its adhesion with the resin. Alternatively, the surface of the chip capacitor may be subjected to silane coupling process.

In the above-described embodiment, the chip capacitors are incorporated in the printed circuit board. Instead of the chip capacitor, it is also possible to use a plate-like capacitor in which a conductive film is formed on a ceramic plate. Needless to say, the structure in which the copper plating is provided and the structure in which the surface of the chip capacitor is roughened as employed in the fourth modification may be applicable to the third embodiment, the first, second, and third modifications of the third embodiment.

(Fifth Modification of Third Embodiment)

The structure of a printed circuit board according to a fifth modification of the third embodiment will be described with reference to Fig. 18.

The printed circuit board according to the fifth modification has the similar structure as of the first modification described above, except for the chip capacitors 20 accommodated in the core substrate 30. Fig. 18 is a plan view showing the chip capacitor. Fig. 18(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 18(A), a chain line shows the cutting line. In the printed circuit board described in the first embodiment, as shown in the plan view of Fig. 18(B), the first electrodes 21 and the second electrodes 22 are provide along the side ends of the chip capacitor. Fig. 18(C) is a diagram showing a chip capacitor before being

cut from which a plurality of pieces are to be obtained by cutting according to the fifth modification. In Fig. 18(C), a chain line shows the cutting line. In the printed circuit board described in the fifth modification, as shown in the plan view of Fig. 18(D), the first electrodes 21 and the second electrodes 22 are provided inside the side ends of the chip capacitor.

In the fifth modification, the printed circuit board has a chip capacitor 20 in which the electrodes are formed inside the side ends thereof. Therefore, a chip capacitor having a large capacity can be used as the chip capacitor 20.

A printed circuit board according to first alternative example of the fifth modification will be described referring to Fig. 19.

Fig. 19 is a diagram showing a plan view of the chip capacitor 20 to be accommodated in the core substrate of the printed circuit board according to a first alternative example. In the above-described first embodiment, a plurality of chip capacitors each having a small capacity are accommodated in the core substrate. Contrary to this, in the first alternative example, a large chip capacitor 20 having a large capacity is accommodated in the core substrate. The chip capacitor 20 includes first electrodes 21, second electrodes 22, a dielectric body 23, a first conductive film 24 connected to the first electrodes 21, a second conductive film 25 connected to the second electrodes 22, and electrodes 27 which are not connected to the first conductive film 24 and the second conductive film 25 and used for connecting the upper and lower surfaces of the chip capacitor. The chip capacitor is connected to the IC chip and the daughter board through the electrodes 27.

In the printed circuit board according to the first alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

Next, a printed circuit board according to a second alternative example will be described referring to Fig. 20. Fig. 20(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 20(A), a chain line shows the cutting line. Fig. 20 (B) is a diagram showing a plan view of the chip capacitor. In the second alternative example, as shown in Fig. 20(B), a plurality of chip capacitors from each of which a plurality of pieces are to be obtained by cutting (in Fig. 20(B), three pieces) are connected into one piece unit having a large size.

In the second alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

In the above-described embodiment, the chip capacitors are incorporated in the printed circuit board. Instead of the chip capacitor, it is also possible to use a plate-like capacitor in which a conductive film is formed on a ceramic plate.

As to the printed circuit board of the fourth modification of the third embodiment, the inductance of

the chip capacitor 420 embedded in the core substrate, and the inductance of the chip capacitor mounted on the back surface of the printed circuit board (on the surface at the side of daughter board) are shown as follows.

5 In the case of a single capacitor:

A capacitor of embedded type: 137pH

A capacitor of back surface mounted type: 287pH

In the case of eight capacitors connected in parallel:

Capacitors of embedded type: 60pH

10 Capacitors of back surface mounted type: 72pH

In both cases where a single capacitor is used and where a plurality of capacitors are connected in parallel to obtain an increased capacity, an inductance can be lowered by incorporating the chip capacitor.

15 Hereinafter, the results of reliability test will be described. In the test, the rate of change in the electrostatic capacity of a single chip capacitor in the printed circuit board of the first embodiment was measured.

20 Rate of change in electrostatic capacity
(measured at a frequency of 100Hz) (measured at a frequency of 1kHz)

Steam 168 hours: 0.3% 0.4%

HAST 100 hours: -0.9% -0.9%

25 TS 1000 cycles: 1.1% 1.3%

In the Steam test, the chip capacitor was subjected to steam to be kept at a moisture of 100%. In the HAST test, the chip capacitor was left for 100 hours at a relative moisture of 100%, an applied voltage of 1.3V, and at a temperature of 121°C. In the TS test, the chip capacitor was tested for 30 minutes at -125°C, and 30 minutes for 55°C, and this test was repeated 1000 times.

In the above-described reliability test, it was realized that the printed circuit board incorporating the chip capacitor attains a reliability of the same level as the conventional printed capacitor on which a capacitor is mounted on its surface. As described above, in the TS test, even if an internal stress is generated due to the difference in the thermal expansion coefficients between the capacitor made of ceramic, and the core substrate and the resin insulating layer made of resin, no problems are created such as a disconnection between the terminal of the chip capacitor and the via holes, a peeling of the chip capacitors from the resin insulating layer, and the cracks in the resin insulating layer. In this manner, high reliability can be attained over a long period of time.

According to the structure of the third embodiment, there is no problem of lowering the electric characteristics caused by inductance.

Since the resin is charged in the space between the core substrate and the capacitors, even if the stress is generated caused by the capacitors, the stress can be alleviated. In addition, no migration is created. As a result, neither peeling nor dissolution is caused between the electrodes of the capacitors and the connecting sections of the via holes. Due to these arrangements, the desired performance can be maintained in the reliability test.

In the case where the electrodes of the capacitors are coated with copper, the generation of migration can be prevented.

(Fourth Embodiment)

The structure of a printed circuit board according to a fourth embodiment of the present invention will be

described with reference to Figs. 51 and 52. Fig. 51 is a diagram showing a cross section of a printed circuit board 610. Fig. 52 is a diagram showing the state where an IC chip 690 is mounted on the printed circuit board 610 shown in Fig. 51, and the printed circuit board 610 is attached to a daughter board 694.

As shown in Fig. 51, the printed circuit board 610 incorporates chip capacitors 620, a core substrate 630 for accommodating chip capacitors 620, and an interlayer resin insulating layer 650 constituting the buildup layers 680A, 680B. The core substrate 630 is constituted by an accommodating layer 630a for accommodating the capacitors 620, and a connection layer 640. Via holes 660 and a conductor circuit 658 are formed in the connection layer 640. Via holes 760 and a conductor circuit 758 are formed in the interlayer resin insulating layer 650. In this embodiment, the buildup layer is constituted by a single interlayer resin insulating layer 650. As an alternative to this, the buildup layer may be constituted by a plurality of interlayer resin insulating layers.

As shown in Fig. 45, the chip capacitor 620 is constituted by a first electrode 621, a second electrode 622, and a dielectric body 623 interposed between the first and second electrodes 621, 622. The dielectric body 623 includes a plurality of first conductive film 624 connected to the first electrode 621 and a plurality of second conductive film 625 connected to the second electrode 622 in an opposed relation to each other.

As shown in Fig. 52, the via holes 760 in the upper buildup layer 680A are formed with bumps 676 to be respectively connected to pads 692S1, 692S2, 692P1, 692P2 of the IC chip 690. On the other hand, the via holes

760 in the lower buildup layer 680B are formed with bumps 676 to be respectively connected to pads 695S1, 695S2, 695P1, 695P2. Through holes 646 are formed in the core substrate 630.

5 The pad 692S2 for signal of the IC chip 690 is connected to the pad 695S2 for signal of the daughter board 694 through the bump 676-the conductor circuit 758-the via hole 760-the through hole 646-and via hole 760-the bump 676. On the other hand, the pad 692S1 for
10 signal of the IC chip 690 is connected to the pad 695S1 for signal of the daughter board 694 through the bump 676- the via hole 760-the through hole 646-via hole 760-bump 676.

 The pad 692P1 for power supply of the IC chip 690
15 is connected to the first electrode 621 of the chip capacitor 620 through the bump 676-via hole 760-the conductor circuit 658-the via hole 660. On the other hand, the pad 695P1 for power supply of the daughter board 694 is connected to the first electrode 621 of the chip
20 capacitor 620 through the bump 676-the via hole 760 the conductor circuit 658 the via hole 660.

 The pad 692P2 for power supply of the IC chip 690 is connected to the second electrode 622 of the chip capacitor 620 through the bump 676-the via hole 760-the
25 conductor circuit 658-the via hole 660. On the other hand, the pad 695P2 for power supply of the daughter board 694 is connected to the second electrode 622 of the chip capacitor 620 through the bump 676-the via hole 760-the conductor circuit 658-the via hole 660.

30 In the printed circuit board 610 of the fourth embodiment, the chip capacitors 620 are placed immediately below the IC chip 690. The distance from the IC chip to each capacitor is shortened, and therefore,

electric power can be instantaneously supplied to the IC chip. That is, the loop length which determines the loop inductance can be shortened.

In addition, the through hole 646 is formed between the chip capacitors 620, and no signal line passes through the chip capacitors 620. In this structure, there is no problem that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and that the transmission is delayed by passing through the high dielectric body.

The external substrate (i.e. daughter board) 694 to be connected to the back surface of the printed circuit board is connected to the first electrode 621 and the second electrode 622 of the capacitor 620 through the via holes 660 formed in the connection layer 640 on the side of IC chip and the via holes 660 formed in the connection layer 640 on the side of daughter board. That is, since the terminals 621, 622 are directly connected to the IC chips 690, and the daughter board 694, the wire length therebetween can be shortened.

In the fourth embodiment, an adhesive 636 is interposed between the side surface of the through opening 637 of the core substrate 630 and the chip capacitor 620. The thermal expansion coefficient of the adhesive 636 is set to the value lower than those of the core substrate 630 and the connection layer 640, that is, are set to the value close to that of the chip capacitor 620 made of ceramics. In this manner, even if internal stress is generated between the core substrate 630 and the connection layer 640, and the chip capacitor 620 caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur in the core substrate and the connection

layer 640. As a result, high reliability can be attained. In addition, the generation of migration can be prevented.

Next, the method for manufacturing the printed circuit board described above referring to Fig. 51 will be described with reference to Figs. 48 to 49.

(1) Prepregs each having a core material impregnated with an epoxy resin are laminated on top of each other to form a laminated plate (i.e. an accommodation layer) 632a, and penetrating openings 637 for accommodating chip capacitors are formed in the laminated plate 632a (Fig. 48(A)). The prepreg 435 may be those generally used in printed circuit board such as prepreg impregnated with, instead of the epoxy resin, BT, phenolic resin, or reinforcement material such as glass cloth. It is also possible to use a resin substrate having no core material such as glass cloth.

It is impossible, however, to use substrates made of ceramic and AlN as the core substrate. These substrates are poor in outer shape processing characteristics, and cannot accommodate capacitors in some cases. In addition, a space is created inside the substrate even if it is filled with a resin.

(2) The chip capacitors 620 are accommodated in the penetrating openings 637 of the accommodation layer 632a (Fig. 48(B)). In this case, it is desirable to peel off the coating 626 from the surface of the first and second electrodes 621, 622 of the chip capacitors 620 in order to increase the connection with the via holes 660 to be formed on the upper layer. It is preferable to interpose an adhesive 636 between the through openings 637 and the chip capacitors 620. As the adhesive 636, it is desirable to use an adhesive having a thermal

expansion coefficient smaller than those of the core substrate and connection layer.

(3) A resin film 640a, the accommodation layer 632a accommodating the chip capacitors 620, and another resin film 640a are laminated on top of one another (Fig. 48(C)). The resin film 640a may be made of, as is the case of the first embodiment, thermosetting resin such as epoxy, BT, polyimide, and olefin, or mixtures of thermosetting resins and thermoplastic resins. In this embodiment, it is preferable to use a film having no core material so that the penetrating openings can be easily formed. In this embodiment, a resin film 640a having no metal layer is laminated. As an alternative to this, a resin film (RCC) having a metal layer on its one side may be used. That is, it is possible to use a both-sided plate, a one-sided plate, a resin plate having no metal film, and a resin film. It is preferable that a resin filler 636a is charged in the upper and lower surfaces of the chip capacitors 620 to increase the air tightness. The resin and interlayer resin insulating layer used in this invention have melting points of 300°C or lower. Therefore, when heat higher than 350°C is applied, the resin and interlayer resin insulating layer may be dissolved, softened, or carbonized.

(4) The accommodation layer 632a and the resin films 640a laminated on top of one another are pressed from both sides to flatten the surface. Then, heating and curing is performed to form a core substrate 630 constituted by an accommodation layer 630a accommodating the chip capacitors 620 and a connection layer 640 (Fig. 49(A)). In this embodiment, the accommodation layer 630a which accommodates the capacitors 620 and the connection

layer 640 are bonded to each other by application of pressure from both sides to form a core substrate 630. As a result, the core substrate 630 has a flat surface. The interlayer resin insulating layer 650 and the conductor circuit 758 can be laminated in a later step in such a manner that high reliability is attained.

(5) Non-penetrating openings 648 to be via holes are formed in the upper connection layer 640 by CO₂ laser, YAG laser, excimer laser, or UV laser (Fig. 49(B)). As the case may be, an areamask on which penetrating openings are formed at positions corresponding to the positions of the non-penetrating openings is mounted, and an area processing is conducted by a laser. In the case where it is desired to form via holes having different sizes and diameter from each other, the lasers may be used in combination to form the via holes.

(6) If necessary, smear in the via holes may be conducted by a gas plasma treatment using a gaseous matter such as oxygen and nitrogen, or dry treatment such as corona treatment, or by immersion into an oxidizer such as permagnetic acid. Subsequently, penetrating openings 646a each having a diameter of 50 to 500 μ m for through holes are penetrated in the core substrate 630 constituted by the connection layer 640, the accommodation layer 630a, and the connection layer 640 by a drill or a laser (Fig. 49(C)).

(7) A metal film is formed on the surface layer of the connection layer 640, the non-penetrating openings 648 for via holes, and the penetrating openings 646a for through holes of the core substrate 630. For this purpose, a palladium catalyst is provided on the surface of the connection layer 640, and then, the core substrate

630 is immersed in an electroless plating solution to uniformly precipitate an electroless copper plated film 652 (Fig. 50(A)). In this embodiment, an electroless plating is employed. Alternatively, a metal film of copper, nickel and the like may be formed by sputtering. The sputtering is disadvantageous from the viewpoint of cost, but is advantageous in that the adhesion with the resin film can be improved. As the case may be an electroless plated film may be formed after the metal layer is formed by sputtering. Depending on the kind of resin, there are cases where the catalyst cannot be stably provided thereto. In this case, the electroless plated film is effective in stably providing the catalyst to such a resin. In addition, the electrolytic plating is more stably precipitated in the case of forming the electroless plated film. The metal film 652 is preferably formed into the thickness of 0.1 to 3mm.

(8) A photosensitive dry film is attached to the surface of the metal film 652, and a mask is placed thereon. Exposure to light and development are performed to form a resist 654 having a predetermined pattern. The core substrate 630 is immersed into an electrolytic plating solution to allow a current to flow in the core substrate 630 through the electroless plated film 652 to precipitate an electrolytic copper plated film 656 (Fig. 50(B)). The resist 654 is peeled by 5% KOH, and then, the electroless plated film 652 below the resist 654 is etched and removed by a mixed solution of sulfuric acid and hydrogen peroxide. As a result, via holes 660 and a conductor circuit 658 are formed in the connection layer 640, and through holes 646 are formed in the penetrating openings 646a of the core substrate 630 (Fig. 50(C)). The subsequent processes are the same as the steps (10)

to (15) of the second embodiment, and therefore, their description will be omitted.

The processes of mounting the IC chip on the printed circuit board, and attaching the printed circuit board to the daughter board are the same as those of the first embodiment, and their description will be omitted. (First Modification of Fourth Embodiment)

Fig. 53 is a diagram showing a printed circuit board according to a first modification of the fourth embodiment. It is also possible, as is the case of the first modification shown in Fig. 53, the first electrode 621 and the second electrode 622 may be connected to the via holes 660 via the adhesive material 634. The conductive adhesive material 634 may be a material having both conductivity and adhesiveness such as a solder (Sn/Pb, Sn/Sb, Sn/Ag), conductive pastes, and resins impregnated with metal particles.

(Second Modification of Fourth Embodiment)

A printed circuit board according to a second modification of the fourth embodiment will be described with reference to Fig. 54. The printed circuit board according to a second modification has a similar structure as of the fourth embodiment, except for the following points. That is, in the printed circuit board of the second modification, conductive pins 696 are provided, and a connection with the daughter board is established through the conductive pins 696.

Whereas in the fourth embodiment described above, chip capacitors 220 are accommodated in the core substrate 630 alone, in the first modification, chip capacitors 720 each having a large capacity are mounted on the front surface and back surface of the core substrate 630, on top of the chip capacitors 620 accommodated in

the core substrate 630.

The IC chip conducts a complicated calculation, and in the calculation processing, it instantaneously consumes a large electric power. In order to provide a large electric power to the IC chip, in this modification, a chip capacitor 620 for power supply and a chip capacitor 720 are provided to the printed circuit board. The effect of providing the chip capacitors 620 and 720 is the same as that attained in the fourth modification of the first embodiment, and therefore, its description will be omitted.

(Third Modification of Fourth Embodiment)

A printed circuit board according to a third modification of the present invention will be described with reference to Fig. 55. A printed circuit board 610 to the third modification has the similar structure as of the fourth embodiment described above, except for the following points. That is, in the printed circuit board 610 according to the third modification, filled vias 660 are formed on a first electrode 621 and a second electrode 622 of chip capacitors 620. The chip capacitors 620 are connected to the bumps 692 of the IC chips 690 through the filled vias 760.

(Fourth Modification of Fourth Embodiment)

A printed circuit board according to a fourth modification of the fourth embodiment will be described with reference to Fig. 56. A printed circuit board 610 according to the fourth modification has the similar structure as of the fourth embodiment described above, except for the following points. That is, in the printed circuit board according to the fourth modification, filled vias 660 are formed on a first electrode 621 and a second electrode 622 of chip capacitors 620. The chip

capacitors 620 are connected to the bumps 692P1, 692P2 of the IC chips 690 through the filled vias 760 formed immediately above the filled vias 660. With this arrangement of the fourth modification, the distance
5 between the IC chip and each chip capacitor can be shortened to the minimum value.

(Fifth Modification of Fourth Embodiment)

A printed circuit board according to a fifth modification of the present invention will be described
10 with reference to Fig. 57. A printed circuit board 610 according to the fifth modification has the similar structure as of the fourth embodiment described above, except for the following points. That is, in the printed circuit board according to the fifth modification, pads
15 on the side of IC chip 690 and the pads 695 on the side of daughter board 694 are connected through a first electrode 621, and a first electrode 622 of the chip capacitors 620. In other words, through holes for power supply and through holes for ground of the IC chip and
20 daughter board are omitted. With this arrangement of the fifth modification, the wiring density can be increased as compared with the case of fourth embodiment.

(Sixth Modification of Fourth Embodiment)

A printed circuit board according to a sixth
25 modification of the fourth embodiment will be described with reference to Figs. 58 and 59.

A printed circuit board according to the sixth modification has the similar structure as of the fourth embodiment described above referring to Fig. 51, except
30 for the following points. That is, in the printed circuit board according to the sixth modification, as shown in Fig. 59, in the chip capacitor 620, the coating layer 626 (see Fig. 45) is completely peeled from the

first and second electrodes 621, 622, and then, the first and second electrodes are coated with a copper plated film 629. An electric connection for the first and second electrodes 621, 622 coated with the copper plated film 629 is established through via holes 660 constituted by copper plating. The electrodes 621, 622 of the chip capacitor are metallized and has pits and projections on their surfaces. If the metal layer is left uncoated and exposed to the outside, the resin may be left in the pits and projections in the step of forming non-penetrating openings 648 in the connection layer 640. The resin left in the pits and projections may cause a disconnection between the first and second electrodes 621, 622 and the via holes 660. Contrary to this, in the sixth modification, the surfaces of the first and second electrodes 621, 622 coated with the copper plated film 629 are flat and smooth. When the non-penetrating openings 648 are formed in the connection layer 640 formed on the electrodes, no resin is left on the surfaces of the electrodes 621, 622. When the via holes 660 are formed, the connection between the via holes 660 and the electrodes 621, 622 has increased reliability.

Since the via holes 660 are made by plating into the electrodes 621, 622 formed with the copper plated film 629, the electrodes 621, 622 are firmly connected to the via holes 660. No disconnection occurs between the electrodes 621, 622 and via holes 660 even when a heat cycle test is conducted.

The copper plated film 629 is formed after a nickel/tin layer (i.e. a coating layer) provided onto the surface of the metal layer 628 constituting the first and first electrodes in the step of manufacturing the chip capacitor is peeled off at the time of mounting the

chip capacitor onto the printed circuit board.

Alternatively, the copper plated film 629 may be directly provided onto the surface of the metal layer 629 in the step of manufacturing the chip capacitor 620. In the sixth modification, as is the case of the fourth embodiment, openings which extend to the copper plated film 629 of the electrodes are formed by a laser, and then a desmear process is performed to form via holes by copper plating. Therefore, even if an oxide film is formed on the surface of the copper plated film 629, the oxide film can be removed in the laser or desmear process. In this manner, the first and second electrodes 621, 622 can be properly connected to the via holes 660.

As is the case of the first embodiment, as shown in Fig. 17(B), the first electrodes 21, 22 of the capacitor 20 may be partially uncoated with the coating 28. When partially uncoated and exposed to the outside, the connection of the first and second electrodes 21, 22 to the via holes 660 can be enhanced.

On the surface of the dielectric body 623 made of ceramic of the chip capacitor 620, a rough surface 623 α is formed. The rough surface 623 α contributes to an increased adhesion between the chip capacitor 620 made of ceramic and the connection layer 640 made of resin, thereby avoiding the connection layer 640 from peeling from the interface with the chip capacitor 620 even when a heat cycle test is conducted. The rough surface 623 α can be formed by polishing the surface of the chip capacitor 620 after the sintering step, or by roughening the surface of the chip capacitor 620 before the sintering step. In the sixth modification, the surface of the chip capacitor is roughened to increase its adhesion with the

resin. Alternatively, the surface of the chip capacitor may be subjected to silane coupling process.

(Seventh Modification of Fourth Embodiment)

5 A structure of a printed circuit board according to a seventh modification of the fourth embodiment will be described referring to Fig. 18.

10 The printed circuit board according to the seventh modification has the structure similar to that of the first embodiment, except for the structure of the chip capacitors 20 accommodated in the core substrate 30. Fig. 18 is a plan view showing the chip capacitors. Fig. 18(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 18(A), a chain line shows the cutting line. In the printed circuit board described in the first embodiment, as shown in the plan view of Fig. 18(B), the first electrodes 21 and the second electrodes 22 are provide along the side ends of the chip capacitor. Fig. 18(C) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting according to the seventh modification. In Fig. 18(C), a chain line shows the cutting line. In the printed circuit board described in the seventh modification, as shown in the plan view of Fig. 18(D), the first electrodes 21 and the second electrodes 22 are provide inside the side ends of the chip capacitor.

In the printed circuit board of the seventh modification, a chip capacitor 20 in which the electrodes are formed inside the side ends thereof is used.

30 Therefore, a chip capacitor having a large capacity can be used as the chip capacitor 20.

A printed circuit board according to a first alternative example of the seventh modification will be

described referring to Fig. 19.

Fig. 19 is a diagram showing a plan view of the chip capacitor 20 to be accommodated in the core substrate of the printed circuit board according to the first alternative example. In the above-described first embodiment, a plurality of chip capacitors each having a small capacity are accommodated in the core substrate. Contrary to this, in the first alternative example, a large chip capacitor having a large capacity is accommodated in the core substrate. The chip capacitor 20 includes first electrodes 21, second electrodes 22, a dielectric body 23, a first conductive film 24 connected to the first electrodes 21, a second conductive film 25 connected to the second electrodes 22, and electrodes 27 which are not connected to the first conductive film 24 and the second conductive film 25 and used for connecting the upper and lower surfaces of the chip capacitor. The chip capacitor is connected to the IC chip and the daughter board through the electrodes 27.

In the printed circuit board according to the first alternative example, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

Next, a printed circuit board according to a second alternative example will be described referring to Fig. 20. Fig. 20(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 20(A), a chain line shows the cutting line. Fig. 20 (B) is a diagram showing

a plan view of the chip capacitor. In the second alternative example, as shown in Fig. 20(B), a plurality of chip capacitors from each of which a plurality of pieces are to be obtained by cutting (in Fig. 20(B), three pieces) are connected into one piece unit having a large size.

In the second alternative example, the chip capacitor 20 has a large size. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle.

In the above-described embodiment, the chip capacitors are incorporated in the printed circuit board. Instead of the chip capacitor, it is also possible to use a plate-like capacitor in which a conductive film is formed on a ceramic plate. Needless to say, the structure in which the copper plating is provided and the structure in which the surface of the chip capacitor is roughened as employed in the sixth modification may be applicable to the fourth embodiment, the first, second, third, fourth, fifth, and sixth modifications.

As to the printed circuit board according to the sixth modification of the fourth embodiment, the inductance of the chip capacitor 620 embedded in the core substrate, and the inductance of the chip capacitor mounted on the back surface of the printed circuit board (on the surface at the side of daughter board) are shown as follows.

In the case of a single capacitor:

A capacitor of embedded type: 137pH

A capacitor of back surface mounted type: 287pH

In the case of eight capacitors connected in parallel:

Capacitors of embedded type: 60pH

Capacitors of back surface mounted type: 72pH

In both cases where a single capacitor is used and where a plurality of capacitors are connected in parallel to obtain an increased capacity, an inductance can be lowered by incorporating the chip capacitor.

Hereinafter, the results of reliability test will be described. In the test, the rate of change in the electrostatic capacity of a single chip capacitor in the printed circuit board of the sixth modification was measured.

Rate of change in electrostatic capacity
(measured at a frequency of 100Hz) (measured at a frequency of 1kHz)

Steam 168 hours:	0.3%	0.4%
HAST 100 hours:	-0.9%	-0.9%
TS 1000 cycles:	1.1%	1.3%

In the Steam test, the chip capacitor was subjected to steam to be kept at a humidity of 100%. In the HAST test, the chip capacitor was left for 100 hours at a relative humidity of 100%, an applied voltage of 1.3V, and at a temperature of 121°C. In the TS test, the chip capacitor was test for 30 minutes at 125°C, and 30 minutes at 55°C, and this test was repeated 1000 times.

In the above-described reliability test, it was realized that the printed circuit board incorporating the chip capacitor attains a reliability of the same level as the conventional printed capacitor on which a capacitor is mounted on its surface. As described above, in the TS test, even if an internal stress is generated due to the difference in the thermal expansion coefficients between the capacitor made of ceramic, and

the core substrate and the resin interlayer insulating layer made of resin, no problems are created such as a disconnection between the terminals of the chip capacitors and the via holes, and peeling of the chip capacitors from the interlayer resin insulating layer, and creation of cracks in the interlayer resin insulating layer. In this manner, high reliability can be attained over a long period of time.

According to the structure of the fourth embodiment, there is no problem of lowering the electric characteristics caused by inductance.

The connection to the capacitors can be established from their bottom surfaces. It can be said that this structure contributes to a shortened loop inductance and an increased degree of freedom.

Since the resin is charged in the space between the core substrate and the capacitor, even if the stress caused by the capacitors is generated, the stress can be alleviated. In addition, no migration is created. As a result, neither peeling nor dissolution is caused between the electrodes of the capacitors and the connecting sections of the via holes. Due to these arrangements, the desired performance can be maintained in the reliability test. In the case where the capacitor is coated with copper, the generation of migration can be prevented.

(Fifth Embodiment)

First, the structure of a printed circuit board according to a fifth embodiment of the present invention will be described with reference to Figs. 63 and 64. Fig. 63 is a diagram showing a cross section of a printed circuit board 810. Fig. 64 is a diagram showing the state where an IC chip 890 is mounted on the printed circuit board

810 shown in Fig. 63, and the printed circuit board 810 is attached to a daughter board 894.

As shown in Fig. 63, the printed circuit board 810 incorporates chip capacitors 820, a core substrate 830 for accommodating the chip capacitors 820, and an interlayer resin insulating layer 850 constituting the buildup layers 880A, 880B. The core substrate 830 is constituted by an accommodating layer 830a for accommodating the capacitor 820, and a connection layer 840. Via holes 860 and a conductor circuit 858 are formed in the connection layer 840. Via holes 960 and a conductor circuit 958 are formed in the interlayer resin insulating layer 850. In this embodiment, the buildup layer is constituted by a single interlayer resin insulating layer 850. As an alternative to this, the buildup layer may be constituted by a plurality of interlayer resin insulating layers.

As shown in Fig. 66(A), the chip capacitor 820 is constituted by a first electrode 821, a second electrode 822, and a dielectric body 823 interposed between the first and second electrodes. The dielectric body 823 includes a plurality of first conductive films 824 connected to the first electrode 821 and a plurality of second conductive films 825 connected to the second electrode 822 in an opposed relation to each other. The first electrode 821 and the second electrode 822 are respectively coated with a metal layer 826 metallized with copper, and further coated with a coating layer 828 such as solder on the metal layer 826. In this embodiment, a connection for the first electrode 821 and the second electrode 822 is established by via holes 860 made of plating. In the printed circuit board according to the fifth embodiment, as shown in Fig. 66(B), the metal layer

826 is exposed from the coating layer 828 formed on the first and second electrodes 821, 822. With this arrangement, as shown in Fig. 63, the connection between the first and second electrodes 821, 822 and the via holes 860 is increased, and the connection resistance therebetween can be lowered.

On the surface of the dielectric body 823 made of ceramic of the chip capacitor 820, a rough surface 823 α is formed. The rough surface 823 α contributes to an increased adhesion between the chip capacitor 820 made of ceramic and the connection layer 840 made of resin, thereby avoiding the connection layer 840 from peeling from the interface with the chip capacitor 820 even when a heat cycle test is conducted. The rough surface 823 α can be formed by polishing the surface of the chip capacitor 820 after the sintering step, or by roughening the surface of the chip capacitor 20 before the sintering step.

As shown in Fig. 64, the via holes 960 in the upper buildup layer 880A are formed with bumps 876 to be respectively connected to pads 892S1, 892S2, 892P1, 892P2 of the IC chip 890. On the other hand, the via holes 960 in the lower buildup layer 880B are formed with bumps 876 to be respectively connected to pads 895S1, 895S2, 895P1, 895P2. Through holes 846 are formed in the core substrate 830.

The pad 892S2 for signal of the IC chip 890 is connected to the pad 895S2 for signal of the daughter board 894 through the bump 876-the conductor circuit 958-the via hole 960-the through hole 846-the via hole 960-the bump 876. On the other hand, the pad 892S1 for signal of the IC chip 890 is connected to the pad 895S1

for signal of the daughter board 894 through the bump 876- the via hole 960-the through hole 846-the via hole 960-the bump 876.

The pad 892P1 for power supply of the IC chip 890 is connected to the first electrode 821 of the chip capacitor 820 through the bump 876-via hole 960-the conductor circuit 858-the via hole 860. On the other hand, the pad 895P1 for power supply of the daughter board 894 is connected to the first electrode 821 of the chip capacitor 820 through the bump 876-the via hole 960-the through hole 846-the conductor circuit 858-the via hole 860.

The pad 892P2 for power supply of the IC chip 890 is connected to the second electrode 822 of the chip capacitor 820 through the bump 876-the via hole 960-the conductor circuit 858-the via hole 860. On the other hand, the pad 895P2 for power supply of the daughter board 894 is connected to the second electrode 822 of the chip capacitor 820 through the bump 876-the via hole 960-the through hole 846-the conductor circuit 858-the via hole 860.

In the printed circuit board 810 of this embodiment, the chip capacitors 820 are placed immediately below the IC chip 890. The distance from the IC chip to each capacitor is shortened, and therefore, electric power can be instantaneously supplied to the IC chip. That is, the loop length which determines the loop inductance can be shortened.

In addition, the through hole 846 is formed between the chip capacitors 820, and no signal line passes through the chip capacitors 820. In this structure, there is no problem that the impedance becomes discontinuous by the high dielectric body to generate a reflection, and

that the transmission is delayed by passing through the high dielectric body.

The external substrate (i.e. daughter board) 894 to be connected to the back surface of the printed circuit board is connected to the first electrode 821 and the second electrode 822 of the capacitor 820 through the via holes 860 formed in the connection layer 840 on the side of IC chip and the through holes 846 formed in the core substrate 830. That is, although the accommodation layer 830a having a core material is hard to process, though holes are formed in the accommodation layer 830a so that the terminals of the capacitors are not directly connected to the outside surface. As a result, the reliability of the connection can be increased.

In this embodiment, as shown in Fig. 63, an adhesive 836 is interposed between the lower surface of the penetrating openings 837 of the core substrate 830 and the chip capacitor 820. In addition, a resin filling agent 836a is charged in a space between the side surface of the penetrating openings 837 and the chip capacitor 820. The thermal expansion coefficients of the resin layer 836 and the resin filling agent 836a provided on the bottom surface of the chip capacitor 820 are set to the values lower than those of the core substrate 830 and the connection layer 840, that is, are set to the values close to that of the chip capacitor 820 made of ceramics. In this manner, even if internal stress is generated between the core substrate 830 and the connection layer 840, and the chip capacitor 820 caused by the difference in the thermal expansion coefficients therebetween, cracks and peelings do not easily occur in the core substrate and the connection layer 840. As a result, high reliability can be attained. In addition,

the generation of migration can be prevented.

The process of manufacturing the printed circuit board of the fifth embodiment will be described with reference to Figs. 60 to 63.

5 (1) Four prepregs 835 impregnated with an epoxy resin are laminated on top of each other to form a laminated plate 832a, and a penetrating opening 837 for accommodating a chip capacitor is formed in the laminated plate 832a. On the other hand, two prepregs 835 are
10 laminated on top of each other to form a laminated plate 832b (Fig. 60(A)). The prepreg 835 may be impregnated with, instead of the epoxy resin, BT, phenolic resin, or reinforcement material such as glass cloth. It is impossible, however, to use substrates made of ceramic and AlN as the core substrate. These substrates are poor
15 in outer shape processing characteristics, and cannot accommodate capacitors in some cases. In addition, a space is created inside the substrate even if it is filled with a resin. The laminated plate 832a and the laminated
20 plate 832b are laminated to each other to form an accommodation layer 830a. Then, as described above referring to Fig. 66(B), chip capacitors 820 from which a coating layer 828 on the first and second electrodes 821, 822 is peeled are accommodated (Fig. 60(B)). It is
25 preferable that an adhesive 836 is interposed between the penetrating openings 837 and the chip capacitor 820. The resin and interlayer resin insulating layer used in this invention has melting points of 300°C or lower. Therefore, when heat higher than 350°C is applied, the
30 resin and interlayer resin insulating layer may be dissolved, softened, or carbonized.

(2) The resin film 840a (i.e. a connection layer)

is laminated on both sides of the accommodating layer constituted by the laminated plate 832a and the laminated plate 832b and accommodating the chip capacitors 820 (Fig. 60(C)), and are pressed from both sides to flatten the surface. Then, heating and curing is conducted to form a core substrate 830 constituted by the accommodating layer 830a accommodating the chip capacitors 820 and the connection layer 840 (Fig. 60(D)). In this embodiment, the accommodating layer 830a which accommodates the capacitors 820 and the connection layer 840 are bonded to each other by application of pressure from both sides to form the core substrate 830. As a result, the core substrate 830 has a flat surface. The interlayer resin insulating layer 850 and the conductor circuit 958 can be laminated in a later step in such a manner that high reliability is attained.

(3) It is preferable that a resin filling agent 836a is charged in the side surface of the penetrating openings 837 of the core substrate to increase the air tightness. In this embodiment, the resin film 840a may be a resin film of the same type as that used in the first embodiment which has no metal layer. As an alternative to this, a resin film (RCC) having a metal layer on its one side may be used. That is, it is possible to use a both-sided plate, a one-sided plate, a resin plate having no metal film, and a resin film.

(4) Penetrating openings 846a each having a diameter of 300 to 500 μ m for through hole are formed in the core substrate and the interlayer resin insulating layer 850 with a drill (Fig. 61(A)). Non-penetrating openings 848 extending to the first and second electrodes 821, 822 are formed in the upper interlayer resin

insulating layer 850 by CO2 laser, YAG laser, excimer laser, or UV laser (Fig. 61(B)). As the case may be, an area mask on which through holes are penetrated at positions corresponding to the positions of the non-penetrating openings is mounted, and an area processing is conducted by a laser. In the case where it is desired to form via holes having different sizes and diameter from each other, the lasers may be used to form the via holes.

(5) A desmear process is performed. Subsequently, a palladium catalyst is provided to the substrate 830, and then, the core substrate 830 is immersed into an electroless plating solution to cause the electroless plated film to uniformly precipitate an electroless plated film 852 (Fig. 61(C)). As a result of this, a rough layer can be formed on the surface of the electroless copper plated film 852. The rough surface has Ra (mean roughness height) of 0.01 to 5 μ m, and especially preferable is Ra of 0.5 to 3 μ m.

(6) A photosensitive dry film is attached on the surface of the electroless plated film 852, and a mask is mounted thereon. Exposure to light and development are performed to form a resist 854 having a predetermined pattern (Fig. 62(A)). In this embodiment, an electroless plating is employed. Alternatively, a metal film of copper, nickel and the like may be formed by sputtering. The sputtering is disadvantageous from the viewpoint of cost, but is advantageous in that the adhesion with the resin film can be improved. The core substrate 830 is immersed in an electrolytic plating solution, and a current is allowed to flow in the core substrate 830 through the electroless plated film 852

to precipitate an electrolytic copper plated film 856 (Fig. 62(B)). The resist 854 is peeled by 5% KOH, and the electroless plated film 852 below the resist 854 is etched with a mixed solution of sulfuric acid and hydrogen peroxide to be dissolved and removed. As a result, via holes 860 are formed in the non-penetrating openings 848 of the connection layer 840, a conductor circuit 858 is formed on the surface of the connection layer 840, and through holes 846 are formed in the penetrating openings 846a of the core substrate 830 (Fig. 62(C)). The subsequent processes are the same as the steps (10) to (15) of the second embodiment which has been described above, and therefore, their description will be omitted.

The processes of mounting the IC chip on the printed circuit board, and attaching the printed circuit board to the daughter board are the same as those of the first embodiment, and their description will be omitted. (First Modification of Fifth Embodiment)

A printed circuit board according to a first modification of the fifth embodiment of this invention will be described with reference to Fig. 65. In the printed circuit board of the first modification, conductive pins 896 are provided, and a connection with the daughter board is established through the conductive pins 896. A core substrate 830 is constituted by an accommodation layer 830a having penetrating opening 837, and connection layers 840 provided on both sides of the accommodation layer 830a. Via holes 860 for establishing connection between the electrodes 821, 822 of the chip capacitors 820 and the IC chip 890 and the conductive pins 896 are formed in the connection layers 840 provided on both sides of the accommodation layer 830a. In this first modification, as shown in Fig. 66(C), the coating of the

electrodes 821, 822 of the chip capacitors 820 is completely removed.

Whereas in the fifth embodiment described above, chip capacitors 820 are accommodated in the core substrate 830 alone, in the first modification, chip capacitors 920 each having a large capacity are mounted on the front surface and back surface of the core substrate 830.

The IC chip conducts a complicated calculation, and in the calculation processing, it instantaneously consumes a large electric power. In order to provide a large electric power to the IC chip, in the first modification, chip capacitors 820 for power supply and chip capacitors 920 are provided to the printed circuit board. The effect of providing the chip capacitors 820 and 920 is the same as that attained in the fourth modification of the first embodiment, and therefore, its description will be omitted.

(Second Modification of Fifth Embodiment)

A printed circuit board according to a second modification of the fifth embodiment will be described referring to Figs. 67 and 68.

The printed circuit board according to the second modification has the similar structure as of the fifth embodiment described above, except for the following points. That is, in the fifth embodiment, the coating of the electrodes 821, 822 of the chip capacitors 820 is partially peeled off to cause the surface of the metal layer 826 to be uncoated and exposed to the outside. Contrary to this, in the printed circuit board according to the second modification, in the chip capacitor 820, as shown in Fig. 68(A), the coating of the metal layer 826 is completely peeled, and then as shown in Fig. 68(B), a copper plated film 829 is coated on the surface of the

metal layer 826. The coating of the plated film may be made of plating such as electrolytic plating and electroless plating. An electric connection for the first and second electrodes 821, 822 coated with the copper plated film 829 is established through via holes 860 constituted by a copper plating. The electrodes 821, 822 of the chip capacitor are metallized and has pits and projections on their surfaces. Therefore, the resin may be left in the pits and projections in the step of forming non-penetrating openings 848 in the connection layer 840 of the fifth embodiment shown in Fig. 61(B). The resin left in the pits and projections may cause a disconnection between the first and second electrodes 821, 822 and the via holes 860. Contrary to this, in the second modification, the surfaces of the first and second electrodes 821, 822 coated with the copper plated film 829 are flat and smooth. When the penetrating openings 848 are formed in the connection layer 840 formed on the electrodes, no resin is left on the surfaces of the electrodes 821, 822. When the via holes 860 are formed, the connection between the via holes 860 and the electrodes 821, 822 has increased reliability.

Since the via holes 860 are made by plating into the electrodes 821, 822 formed with the copper plated film 829, the electrodes 821, 822 are firmly connected to the via holes 860. No disconnection occurs between the electrodes 821, 822 and via holes 860 even when a heat cycle test is conducted.

The copper plated film 829 is formed after removing the coating layer 828 in the step of accommodating the chip capacitors in the printed circuit board. Alternatively, the copper plated film 829 may be directly provided onto the surface of the metal layer 826 in the

step of manufacturing the chip capacitor 820. In the second modification, openings which extend to the copper plated film 829 of the electrodes are formed by a laser, and then a desmear process is performed to form via holes by copper plating. Therefore, even if an oxide film is formed on the surface of the copper plated film 829, the oxide film can be removed in the laser or desmear process. In this manner, the first and second electrodes 821, 822 can be properly connected to the via holes 860.

On the surface of the dielectric body 823 made of ceramic of the chip capacitor 820, a rough surface 823 α may be formed. The rough surface 823 α contributes to an increased adhesion between the chip capacitor 820 made of ceramic and the connection layer 840 made of resin, thereby avoiding the connection layer 840 from peeling from the interface with the chip capacitor 820 even when a heat cycle test is conducted. (Third Modification of Fifth Embodiment)

A structure of a printed circuit board according to a third modification of the fifth embodiment will be described referring to Figs. 69 and 18.

The printed circuit board 810 according to the third modification has the structure similar to that of the fifth embodiment, except for the structure of the chip capacitors 20 accommodated in the core substrate 830. Fig. 18 is a plan view showing the chip capacitors. Fig. 18(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 18(A), a chain line shows the cutting line. In the printed circuit board described in the third modification, as shown in the plan view of Fig. 18(B), the first electrodes 21 and the second

electrodes 22 are provide along the side ends of the chip capacitor. Fig. 18(C) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting according to the third modification. In Fig. 18(C), a chain line shows the cutting line. In the printed circuit board described in the third modification, as shown in the plan view of Fig. 18(D), the first electrodes 21 and the second electrodes 22 are provide inside the side ends of the chip capacitor.

In the third modification, the printed circuit board has a chip capacitor 20 in which the electrodes are formed along an inside of the outer edge thereof. Therefore, a chip capacitor having a large capacity can be used as the chip capacitor 20. In the third modification, the surface of the chip capacitors are subjected to roughening process.

(Fourth Modification of Fifth Embodiment)

A printed circuit board according to a fourth modification of the present invention will be described referring to Figs. 70 and 19.

Fig. 70 is a diagram showing a cross section of a printed circuit board 810 according to the fourth modification. Fig. 68 is a diagram showing a plan view of the chip capacitor 20 to be accommodated in the core substrate 830 of the printed circuit board 810. In the above-described fifth embodiment, a plurality of chip capacitors each having a small capacity are accommodated in the core substrate. Contrary to this, in the fourth modification, a large chip capacitor 20 having a large capacity and having electrodes formed in matrix is accommodated in the core substrate 830. The chip capacitor 20 includes first electrodes 21, second

electrodes 22, a dielectric body 23, a first conductive film 24 connected to the first electrodes 21, a second conductive film 25 connected to the second electrodes 22, and electrodes 27 which are not connected to the first conductive film 24 and the second conductive film 25 and used for connecting the upper and lower surfaces of the chip capacitor. The chip capacitor is connected to the IC chip and the daughter board through the electrodes 27.

In the printed circuit board according to the fourth modification, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board even if the printed circuit board is repeatedly subjected to heat cycle. In the fourth modification, the surface of the chip capacitors are subjected to roughening process. (Fifth Modification of Fifth Embodiment)

A printed circuit board according to a fifth modification will be described referring to Figs. 71 and 20. Fig. 71 is a diagram showing a cross section of the printed circuit board. Fig. 20(A) is a diagram showing a chip capacitor before being cut from which a plurality of pieces are to be obtained by cutting. In Fig. 20(A), a chain line shows an ordinary cutting line. Fig. 20 (B) is a diagram showing a plan view of the chip capacitor. As shown in Fig. 20(B), a plurality of chip capacitors from each of which a plurality of pieces are to be obtained by cutting (in Fig. 20(B), three pieces) are connected into one piece unit having a large size.

In the fifth modification, the chip capacitor 20 having a large size is used. Therefore, a chip capacitor

having a large capacity can be employed as the chip capacitor 20. In addition, the use of large-sized chip capacitor 20 prevents the warpage of the printed circuit board 810 even if the printed circuit board is repeatedly subjected to heat cycle. In the fifth modification, the surface of the chip capacitors are subjected to roughening process.

(Sixth Modification of Fifth Embodiment)

A printed circuit board according to a sixth modification will be described with reference to Fig. 72. Fig. 72 is a diagram showing a cross section of the printed circuit board. In the fifth modification described referring to Fig. 63, one chip capacitor 820 is accommodated in the cavity 832 of the core substrate 830. Contrary to this, in the sixth modification, a plurality of chip capacitors 820 are accommodated in the cavity 832. In the sixth modification, the chip capacitors can be incorporated in the core substrate with high density. In the sixth modification, the surface of the chip capacitors is subjected to roughening process.

In the above-described embodiment, the chip capacitor is incorporated in the printed circuit board. Instead of the chip capacitor, it is also possible to use a plate-like capacitor in which a conductive film is formed on a ceramic plate. In this embodiment, the surface of the chip capacitor is roughened to increase its adhesion with the resin insulating layer. Alternatively, the surface of the chip capacitor may be subjected to silane coupling process.

As to the printed circuit board of the second modification, the inductance of the chip capacitor 20 embedded in the core substrate, and the inductance of the chip capacitor mounted on the back surface of the

printed circuit board (on the surface at the side of daughter board) are shown as follows.

In the case of a single capacitor:

A capacitor of embedded type: 137pH

5 A capacitor of back surface mounted type: 287pH

In the case of eight capacitors connected in parallel:

Capacitors of embedded type: 60pH

Capacitors of back surface mounted type: 72pH

10 In both cases where a single capacitor is used and where a plurality of capacitors are connected in parallel to obtain an increased capacity, an inductance can be lowered by incorporating the chip capacitor.

Hereinafter, the results of reliability test will be described. In the test, the rate of change in the electrostatic capacity of a single chip capacitor in the printed circuit board of the second modification was measured.

Rate of change in electrostatic capacity
(measured at a frequency of 100Hz) (measured at a frequency of 1kHz)

Steam 168 hours:	0.3%	0.4%
HAST 100 hours:	-0.9%	-0.9%
TS 1000 cycles:	1.1%	1.3%

25 In the Steam test, the chip capacitor was subjected to steam to be kept at a humidity of 100%. In the HAST test, the chip capacitor was left for 100 hours at a relative humidity of 100%, an applied voltage of 1.3V, and at a temperature of 121°C. In the TS test, the chip capacitor was left for 30 minutes at 125°C, and 30 minutes at 55°C, and this test was repeated 1000 times.

In the above-described reliability test, it was realized that the printed circuit board incorporating

the chip capacitor attains a reliability of the same level as the conventional printed capacitor on which a capacitor is mounted on its surface. As described above, in the TS test, even if an internal stress is generated due to the difference in the thermal expansion coefficients between the capacitor made of ceramic, and the core substrate and the interlayer resin insulating layer made of resin, no problems are created such as a disconnection between the terminals of the chip capacitors and the via holes, a peeling of the chip capacitors from the interlayer resin insulating layer, and the cracks in the interlayer resin insulating layer. In this manner, high reliability can be attained over a long period of time.

According to the structure of the fifth embodiment, there is no problem of lowering the electric characteristics caused by inductance.

Under the conditions of the reliability test, neither deterioration in electric characteristics nor peeling and cracks in the printed circuit board are caused. Therefore, no problems are created between the chip capacitors and the via holes.

Since the resin is charged in the space between the core substrate and the capacitor, even if the stress caused by the capacitors is generated, the stress can be alleviated. In addition, no migration is created. As a result, neither peeling nor dissolution is caused between the electrodes of the capacitors and the connecting sections of the via holes. Due to these arrangements, the desired performance can be maintained in the reliability test.

In the case where the capacitor is coated with copper, the generation of migration can be prevented.

WHAT IS CLAIMED IS:

1. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated on the core substrate, wherein a cavity
5 is formed in the core substrate, and a plurality of capacitors are accommodated in the cavity.

2. A printed circuit board according to claim 1, wherein a resin is charged between the plurality of capacitors in the cavity, and the resin has a thermal
10 expansion coefficient smaller than a thermal expansion coefficient of the core substrate.

3. A printed circuit board according to claim 1 or 2, wherein penetrating openings are formed in the resin layer to form through holes.

4. A printed circuit board according to claim 1 or 2, wherein a metal film is formed on electrodes of the capacitor, and an electric connection for the
15 electrodes formed with the metal film is established by plating.

5. A printed circuit board according to claim 4, wherein the metal film formed on the electrodes of the chip capacitor is a plated film including copper as
20 a main component.

6. A printed circuit board according to claim 1 or 2, wherein at least a part of electrodes of each capacitor is uncoated with a coating layer and exposed
25 to the outside, and an electric connection for the electrode exposed from the coating layer is established by plating.

7. A printed circuit board according to any one of claims 1 to 6, wherein a chip capacitor in which electrodes are formed along an inside of the outer edge
30 thereof is used.

8. A printed circuit board according to any one of claims 1 to 8, wherein a chip capacitor in which electrodes are formed in matrix is used.

9. A printed circuit board according to any one of claims 1 to 8, wherein a capacitor is mounted on the surface of the printed circuit board.

10. A method for manufacturing a printed circuit board, comprising at least the following steps (a) to (c):

- 10 (a) forming a cavity in a core substrate;
- (b) mounting a plurality of capacitors in the cavity; and
- (c) charging a resin between the capacitors.

11. A method for manufacturing a printed circuit board according to claim 6, comprising, after the step (b), a step of applying a pressure to the upper surfaces of the plurality of capacitors in the cavity to align the upper surfaces of the capacitors to the same heights with each other.

12. A method for manufacturing a printed circuit board according to claim 6, comprising, after the step (c), a step of forming penetrating openings in the resin layer to form through holes.

13. A method for manufacturing a printed circuit board comprising at least the following steps (a) to (c):

- 25 (a) forming penetrating openings in a resin material having a core material impregnated with a resin;
- (b) attaching a resin material to the resin material formed with the penetrating openings to form a core substrate having a cavity;
- 30 (c) mounting a plurality of capacitors in the cavity of the core substrate; and
- (d) charging a resin between the capacitors.

14. A method for manufacturing a printed circuit board according to claim 13, comprising, after the step (c), a step of applying a pressure to the upper surfaces of the plurality of capacitors in the cavity to align the upper surfaces of the capacitors to the same heights with each other.

15. A method for manufacturing a printed circuit board according to claim 13, comprising, after the step (d), a step of forming penetrating openings in the resin layer to form through holes.

16. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated on the core substrate,

wherein the core substrate incorporates a connection layer formed by an insulating resin layer including at least one or more layer, and an accommodation layer accommodating a capacitor in its spot-faced section.

17. A printed circuit board according to claim 16, wherein the accommodation layer incorporates a resin substrate having a core material impregnated with a resin, and the connection layer incorporates a resin substrate having no core material.

18. A printed circuit board according to claim 16 or 17, wherein the connection layer and the capacitor is connected to each other through a conductive adhesive.

19. A printed circuit board according to claim 18, wherein the core substrate has a circuit connected to the conductive adhesive between the connection layer and the accommodation layer.

20. A printed circuit board according to claim 17, wherein the IC chip provided on the surface of the printed circuit board is connected to the terminal of

the capacitor through the via holes formed in the connection layer, and

wherein the external substrate provided to the back surface of the printed circuit board is connected to the terminal of the capacitor through the via holes and the through holes formed in the core substrate.

21. A printed circuit board according to any one of claims 16 to 20, wherein a plurality of the capacitors are accommodated, and a wiring for connecting the IC chip to the external substrate is provided between the capacitors.

22. A printed circuit board according to any one of claims 16 to 21, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used.

23. A printed circuit board according to any one of claims 16 to 22, wherein a chip capacitor in which electrodes are formed in matrix is used.

24. A printed circuit board according to any one of claims 16 to 23, wherein a capacitor is mounted on the surface of the printed circuit board.

25. A printed circuit board according to 24, wherein the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board.

26. A printed circuit board according to claim 24, wherein the chip capacitor mounted on the surface of the printed circuit board has an inductance same or larger than the inductance of the chip capacitor incorporated in the printed circuit board.

27. A printed circuit board according to any one of claims 16 to 25, wherein a metal film is formed on

electrodes of the chip capacitor is a plated film including copper as a main component.

28. A printed circuit board according to any one of claims 16 to 26, wherein a resin having a thermal expansion coefficient smaller than the thermal expansion coefficient of the core substrate is charged between the spot-faced section of the core substrate and the chip capacitor.

29. A method for manufacturing a printed circuit board, comprising at least the following steps (a) to (c):

(a) forming a circuit pattern on a resin plate on its one side or both sides, and connecting a capacitor to the circuit pattern through an adhesive material;

(b) attaching a resin substrate formed with a cavity for accommodating the capacitor to the resin plate to form a core substrate; and

(c) forming openings extending to electrodes of the capacitor in the resin plate to form via holes.

30. A method for manufacturing a printed circuit board according to claim 29, wherein, in the attachment step of (c), a pressure is applied to the substrate from its both surfaces.

31. A method for manufacturing a printed circuit board according to claim 29 or 30, comprising, before or after the step of (c), a step of forming penetrating openings in the core substrate constituted by attaching the resin plate to the resin substrate to form through holes.

32. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

wherein the core substrate incorporates a

connection layer formed by an insulating resin layer including at least one or more layer, and an accommodation layer formed by a resin layer accommodating a capacitor and including two or more layers.

5 33. A printed circuit board comprising a resin insulating layer and a conductor circuit laminated to the core substrate,

 wherein the core substrate incorporates a connection layer formed by an insulating resin layer including at least one or more layer, and an accommodation layer formed by a resin layer accommodating a capacitor and including two or more layers, and vias for establishing a connection with the capacitor are formed on both sides of the core substrate.

10 34. A printed circuit board according to claim 33, wherein the via holes formed in the core substrate are made of a metal film formed by one of methods selected from plating, sputtering, and deposition.

15 35. A printed circuit board according to any one of claims 32 to 34, wherein the accommodation layer and the capacitor is bonded to each other by an insulating adhesive.

20 36. A printed circuit board according to any one of claims 32 to 35, wherein a plurality of the capacitors are accommodated, and a wiring for connecting an IC chip and an external substrate to each other is provided between the capacitors.

25 37. A printed circuit board according to any one of claims 32 to 36, a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used.

30 38. A printed circuit board according to any one of claims 32 to 37, wherein a chip capacitor in which

electrodes are formed in matrix is used.

39. A printed circuit board according to any one of claims 32 to 38, wherein a capacitor is mounted on the surface of the printed circuit board.

5 40. A printed circuit board according to 39, wherein the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board.

10 41. A printed circuit board according to claim 39, wherein the chip capacitor mounted on the surface of the printed circuit board has an inductance same or larger than the inductance of the chip capacitor incorporated in the printed circuit board.

15 42. A printed circuit board according to any one of claims 32 to 41, wherein a metal film is formed on electrodes of the chip capacitor, and an electric connection to the electrodes formed with the metal film is established by plating.

20 43. A printed circuit board according to any one of claim 42, wherein a metal film formed on electrodes of the chip capacitor is a plated film including copper as a main component.

25 44. A printed circuit board according to any one of claims 32 to 41, wherein at least a part of electrodes of each capacitor is uncoated with a coating layer and exposed to the outside, and an electric connection for the electrode exposed from the coating layer is established by plating.

30 45. A printed circuit board according to claim 35, wherein the insulating adhesive has a thermal expansion coefficient smaller than the thermal expansion coefficient of the accommodation layer.

46. A method for manufacturing a printed circuit board comprising at least the following steps (a) to (e):

(a) forming penetrating openings for accommodating a capacitor in a first resin material having a core material impregnated with a resin;

(b) attaching a second resin material to the first resin material formed with the penetrating openings to form an accommodation layer having a section for accommodating a capacitor;

(c) accommodating the capacitor in the accommodation layer;

(d) attaching a third insulating resin layer to the accommodation layer formed in the step (c) to form a core substrate; and

(e) forming openings extending to electrodes of the capacitor in the third insulating resin layer to form via holes.

47. A method for manufacturing a printed circuit board comprising at least the following steps (a) to (e):

(a) forming penetrating openings for accommodating a capacitor in a first resin material having a core material impregnated with a resin;

(b) providing a capacitor to the second resin material at a position corresponding to a section for accommodating a capacitor in the resin material;

(c) attaching the first resin material subjected to the step (a) and the second resin material subjected to the step (b) to each other to form an accommodation layer accommodating the capacitor;

(d) attaching a third insulating resin layer to the accommodation layer to form a core substrate; and

(e) forming openings in the third insulating resin layer extending to electrodes of the capacitor to form

via holes.

48. A method for manufacturing a printed circuit board comprising at least the following steps (a) to (f):

5 (a) forming penetrating openings for accommodating a capacitor in a first resin material having a core material impregnated with a resin;

(b) providing a capacitor to the second resin material at a position corresponding to a section for accommodating a capacitor in the resin material;

10 (c) attaching the first resin material subjected to the step (a) and the second resin material subjected to the step (b) to each other to form an accommodation layer accommodating the capacitor;

15 (d) attaching a third insulating resin layer to the accommodation layer to form a core substrate;

(e) forming openings in the third insulating resin layer extending to electrodes of the capacitor to form via holes; and

20 (f) forming a conductive film in the penetrating openings of the first resin material and the openings of the third resin material to form via holes.

49. A method for manufacturing a printed circuit board according to any one of claims 46 to 48, wherein, in the attachment step of (d), a pressure is applied to
25 the substrate from its both surfaces.

50. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

30 wherein the core substrate incorporates an accommodating layer having penetrating openings in each of which a capacitor is accommodated, and connection layers each made of an insulating resin layer and provided on the front surface and the back surface of the

accommodation layer.

51. A printed circuit board according to claim 50, wherein the accommodation layer incorporates a resin substrate having a core material impregnated with a resin, and the connection layer incorporates a resin substrate having no core material.

52. A printed circuit board according to claim 50 or 51, wherein the capacitor is fixed in each of the penetrating openings of the accommodation layer through an insulating adhesive.

53. A printed circuit board according to any one of claim 50 to 52, wherein the connection layers provided on the front surface and the back surface of the accommodation layer are provided with via holes for connecting the connection layers to an IC chip and an external substrate.

54. A printed circuit board according to any one of claims 50 to 53, wherein a plurality of the capacitors are accommodated, and a wiring for connecting the IC chip to the external substrate is provided between the capacitors.

55. A printed circuit board according to any one of claims 50 to 54, wherein a capacitor is mounted on the surface of the printed circuit board.

56. A printed circuit board according to 55, wherein the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor incorporated in the printed circuit board.

57. A printed circuit board according to claim 55, wherein the chip capacitor mounted on the surface of the printed circuit board has an inductance same or larger than the inductance of the chip capacitor

incorporated in the printed circuit board.

58. A printed circuit board according to any one of claims 50 to 55, wherein a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used.

59. A printed circuit board according to any one of claims 50 to 55, wherein a chip capacitor in which electrodes are formed in matrix is used.

60. A printed circuit board according to any one of claims 50 to 59, wherein a metal film is formed on electrodes of the capacitor, and an electric connection for the electrode formed with the metal film is established by plating.

61. A printed circuit board according to claim 60, wherein the metal film formed on electrodes of the chip capacitor is a plated film including copper as a main component.

62. A printed circuit board according to any one of claims 50 to 58, wherein at least a part of electrodes of each capacitor is uncoated with a coating layer and exposed to the outside, and an electric connection for the electrode exposed from the coating layer is established by plating.

63. A printed circuit board according to claim 52, wherein the insulating adhesive has a thermal expansion coefficient smaller than the thermal expansion coefficient of the accommodation layer.

64. A method for manufacturing a printed circuit board comprising at least the following steps (a) to (d):

(a) forming penetrating openings for accommodating a capacitor in a first resin material having a core material impregnated with a resin;

(b) accommodating a capacitor in each of the

penetrating openings of the first resin material;

(c) attaching a second resin material to the first resin material to form a core substrate; and

(d) forming openings extending to electrodes of the capacitor in the second resin material of the core substrate to form via holes.

65. A method for manufacturing a printed circuit board according to claim 64, comprising, before or after the step (d), a step of forming penetrating openings on the core substrate to form through holes.

66. A method for manufacturing a printed circuit board according to claim 64 or 53, wherein, in the attachment step (c), a pressure is applied to the substrate from its both surfaces.

67. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

wherein a capacitor is accommodated in the core substrate.

68. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

wherein the chip capacitor is accommodated in the printed circuit board in the state where at least a part of electrodes of each capacitor is uncoated with a coating layer and exposed to the outside, and an electric connection for the electrode exposed from the coating layer is established by plating.

69. A printed circuit board according to claim 68, wherein the metal film formed on electrodes of the chip capacitor is a plated film including copper as a main component.

70. A printed circuit board comprising a core

substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

wherein the chip capacitor is accommodated in the state where a metal film is formed on electrodes of the capacitor, and an electric connection for the electrodes formed with the metal film is established by plating.

71. A printed circuit board according to claim 70, wherein the metal film formed on electrodes of the chip capacitor is a plated film including copper as a main component.

72. A printed circuit board according to any one of claims 67 to 70, wherein a chip capacitor in which electrodes are formed along an inside of the outer edge thereof is used.

73. A printed circuit board according to any one of claims 67 to 72, wherein a chip capacitor in which electrodes are formed in matrix is used.

74. A printed circuit board according to any one of claims 67 to 73, wherein a plurality of chip capacitors from each of which a plurality of pieces are to be obtained are coupled into one-piece unit, and the one-piece unit is used.

75. A printed circuit board comprising a core substrate, and a resin insulating layer and a conductor circuit laminated to the core substrate,

wherein a capacitor is accommodated in the core substrate, and a capacitor is mounted on the surface of the printed circuit board.

76. A printed circuit board according to 75, wherein the chip capacitor mounted on the surface of the printed circuit board has an electrostatic capacity same or larger than the electrostatic capacity of the chip capacitor in the core substrate.

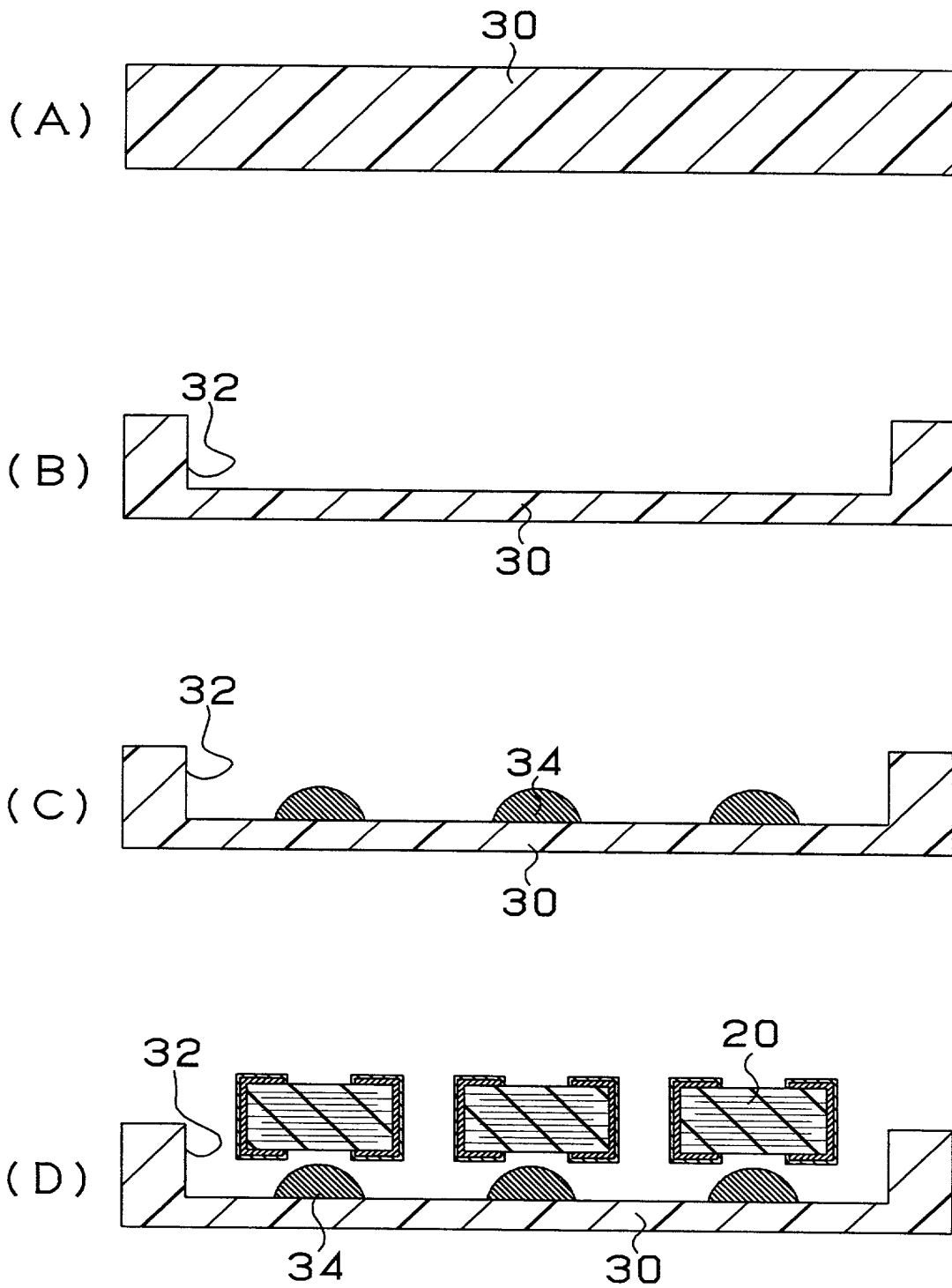
77. A printed circuit board according to claim
75, wherein the chip capacitor mounted on the surface
of the printed circuit board has an inductance same or
larger than the inductance of the chip capacitor
5 incorporated in the printed circuit board.

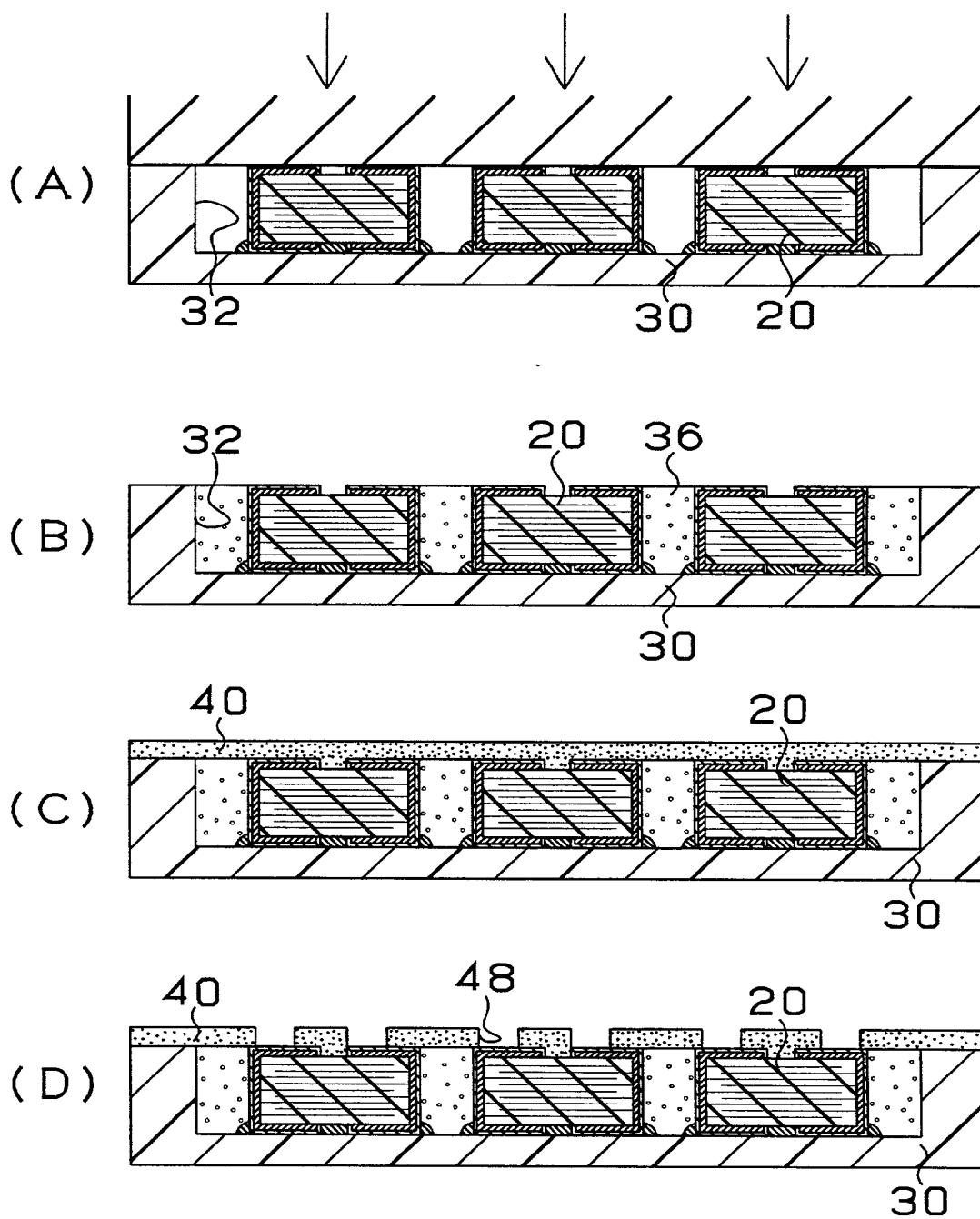
78. A capacitor to be incorporated in a printed
circuit board, wherein a copper plated film is coated
on the surface of a metallized electrodes of a chip
capacitor.

10

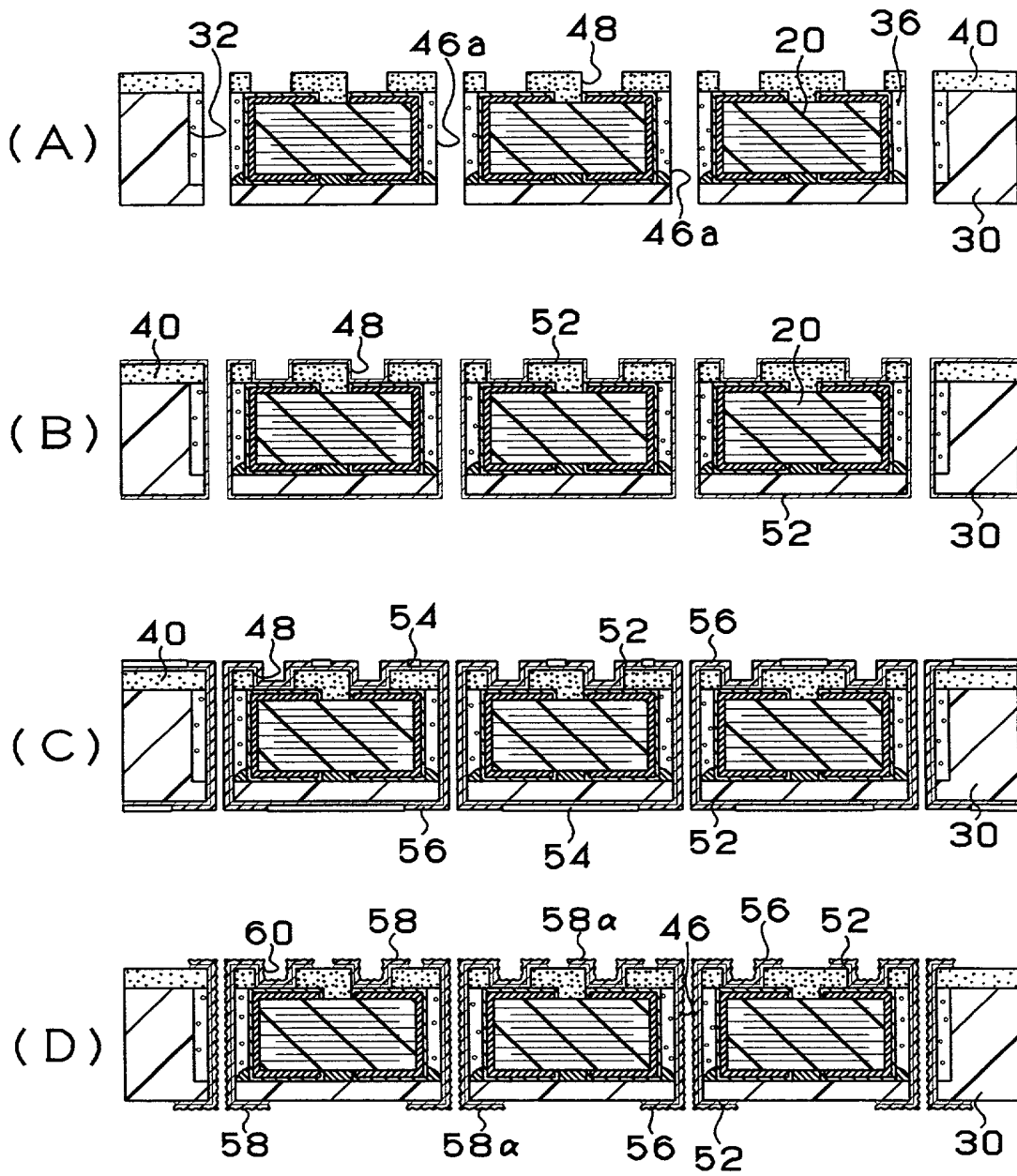
Abstract

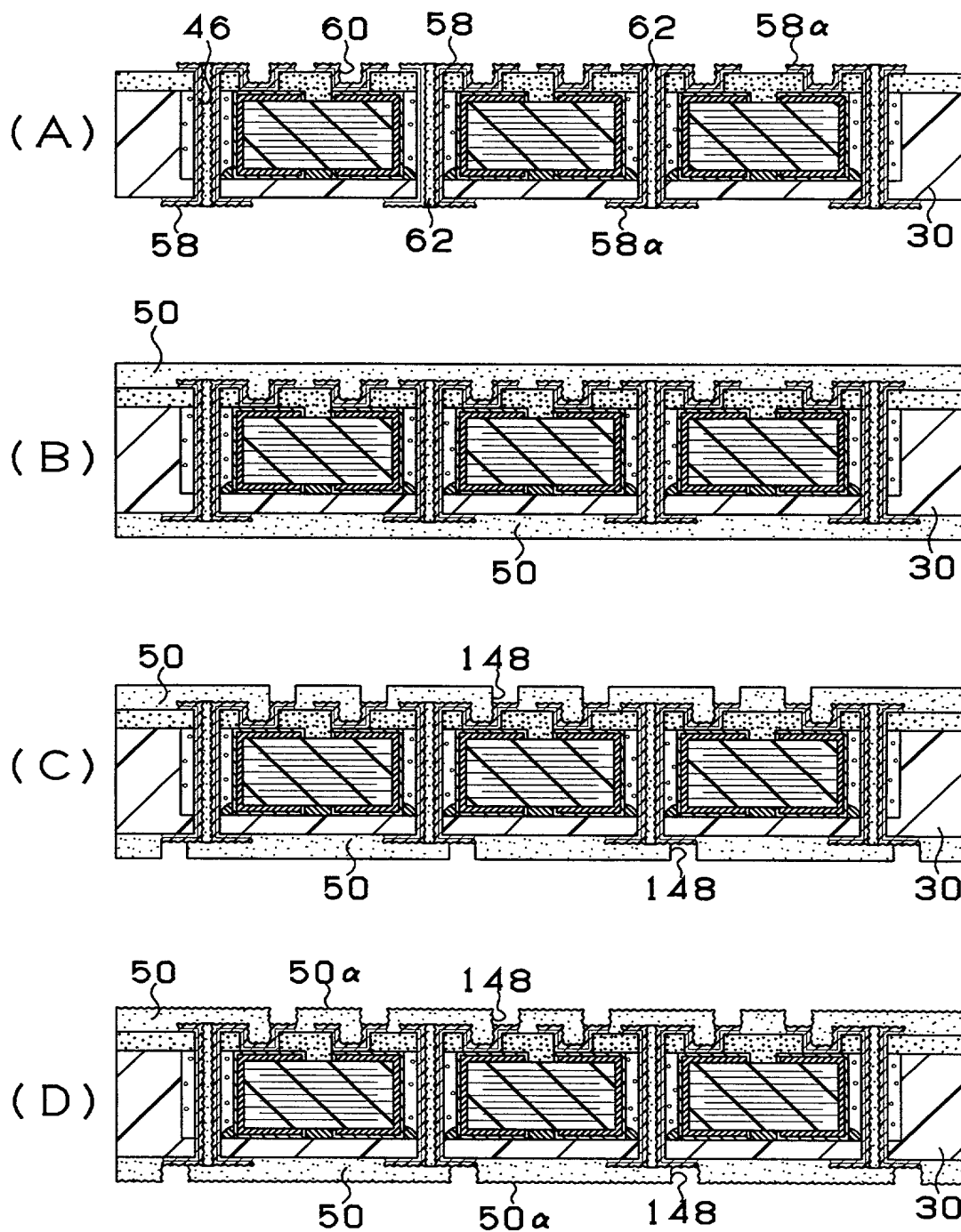
Chip capacitors 20 are provided in a printed circuit board 10. In this manner, the distance between an IC chip 90 and each chip capacitor 20 is shortened, and the loop inductance is reduced. In addition, the chip capacitors 20 are accommodated in a core substrate 30 having a large thickness. Therefore, the thickness of the printed circuit board does not become large.

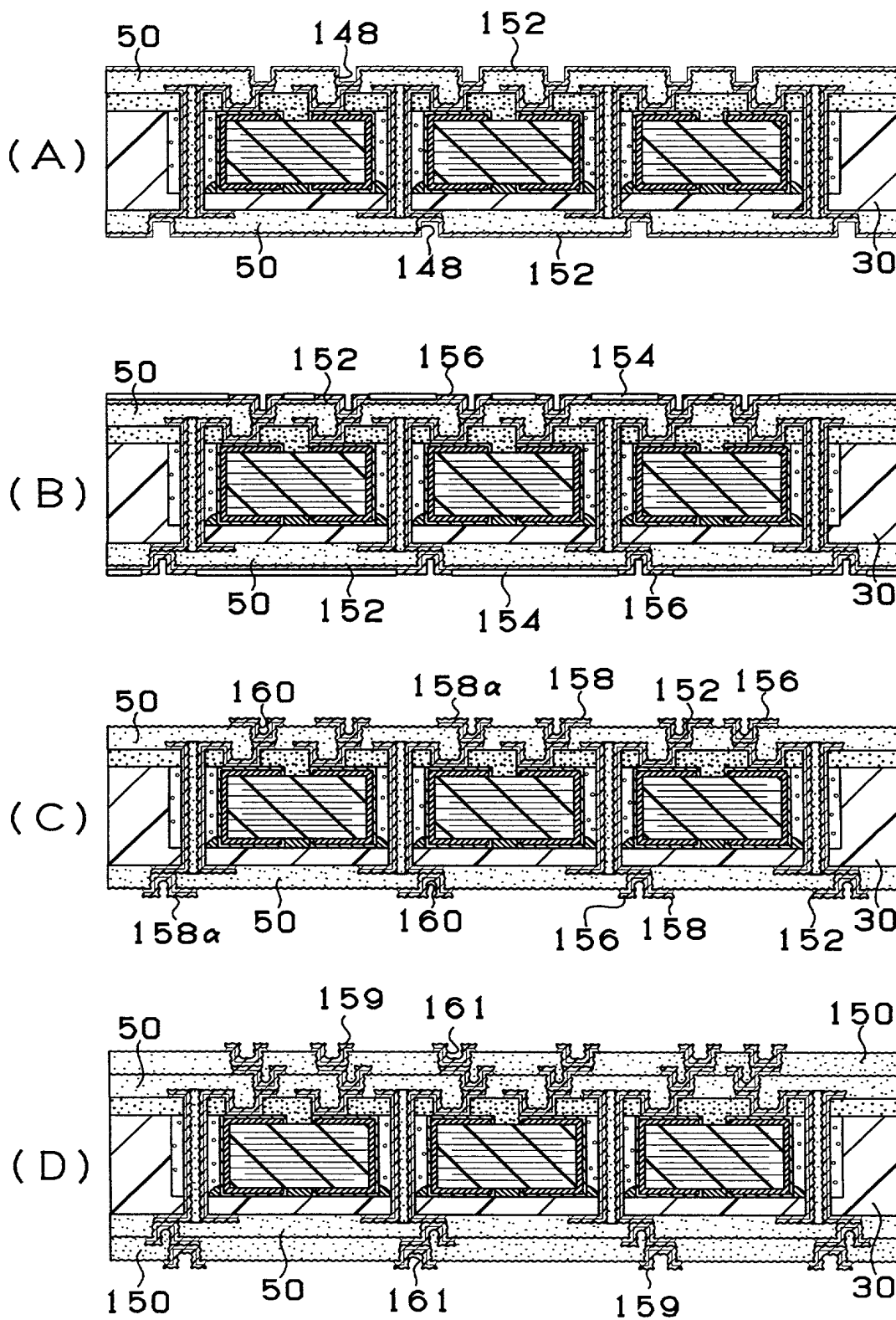
1/73
Fig. 1

2/73
Fig. 2

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Fig. 3

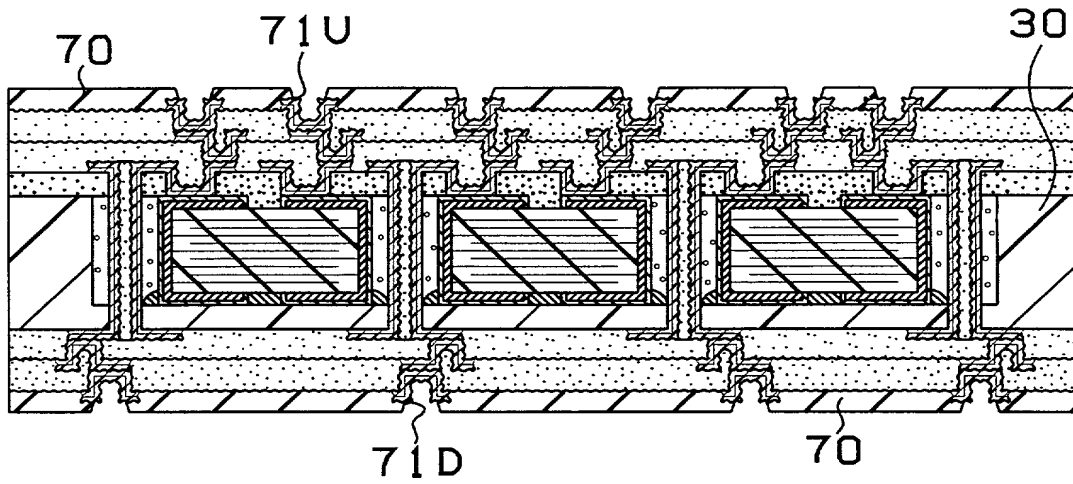


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Fig. 4

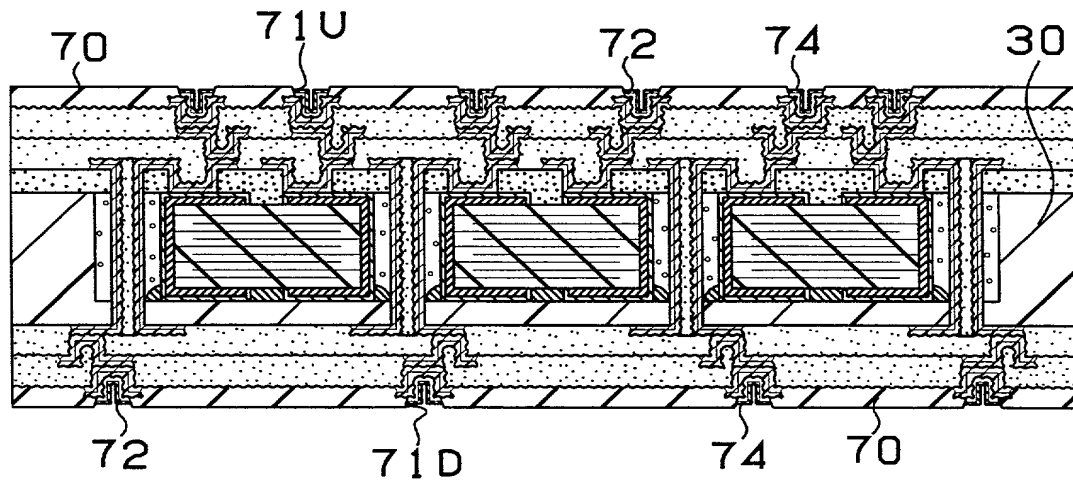
5/73
Fig. 5

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Fig. 6

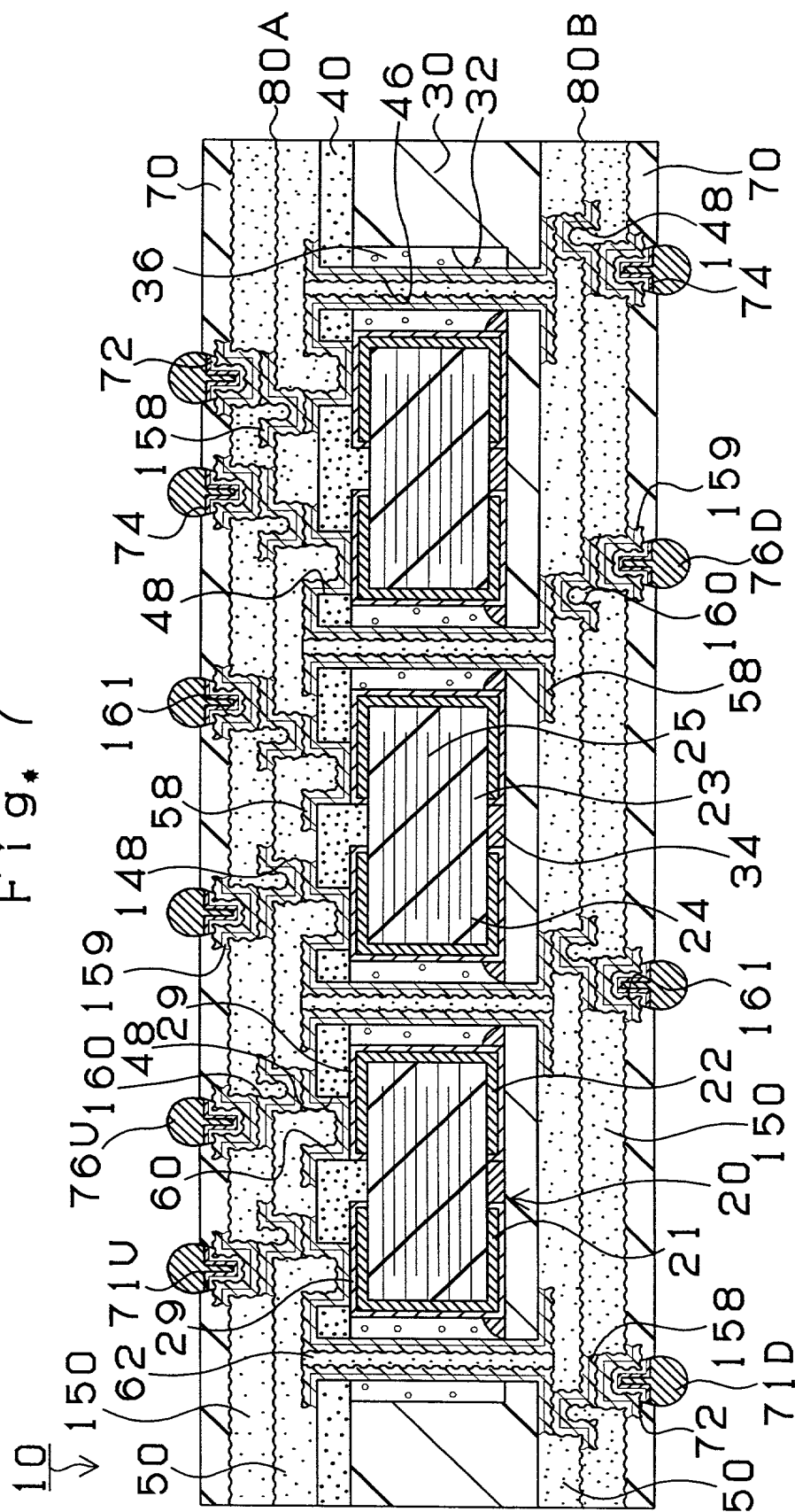
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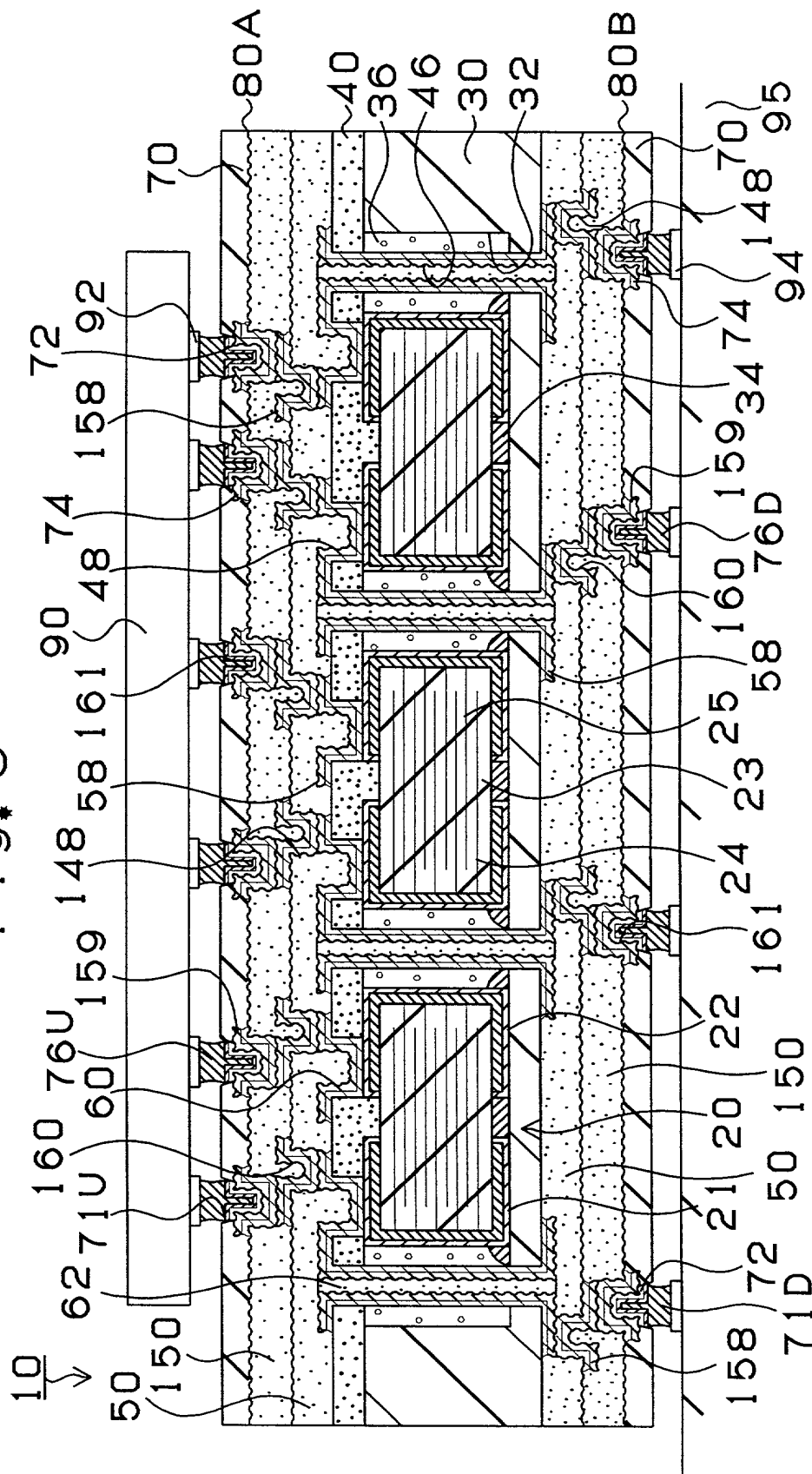
(B)



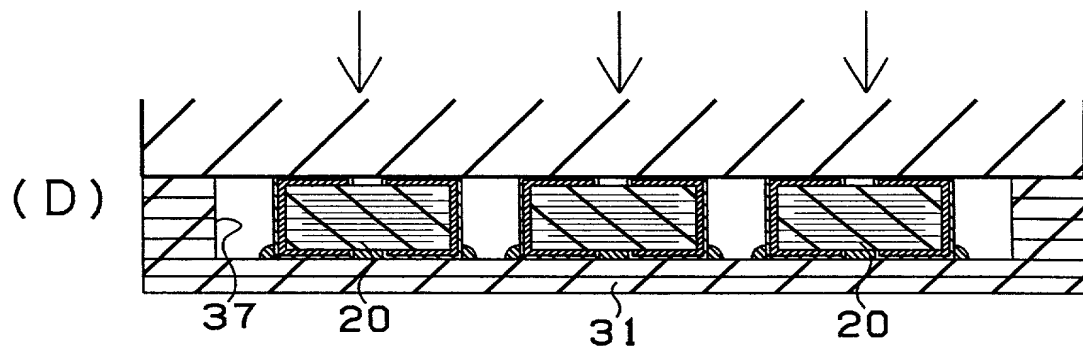
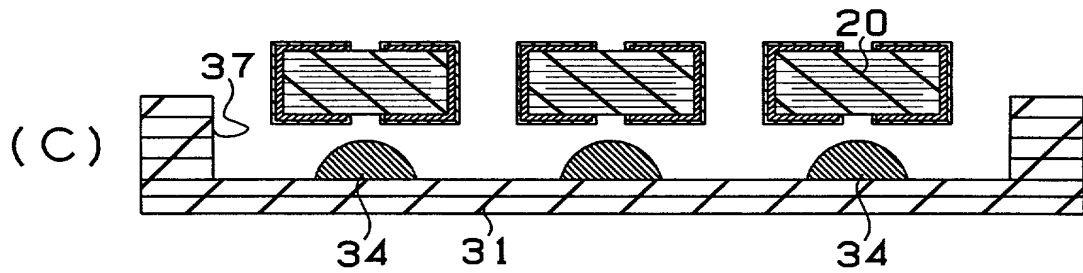
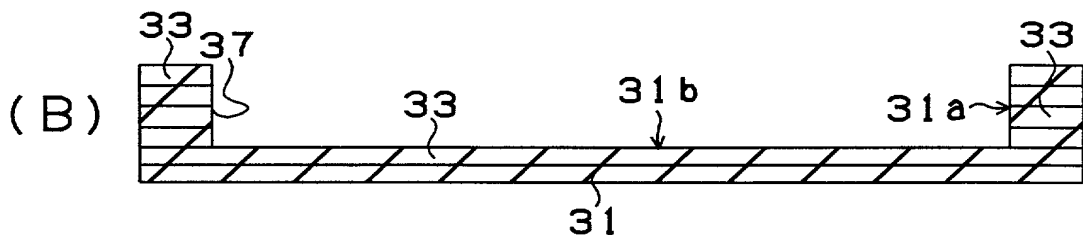
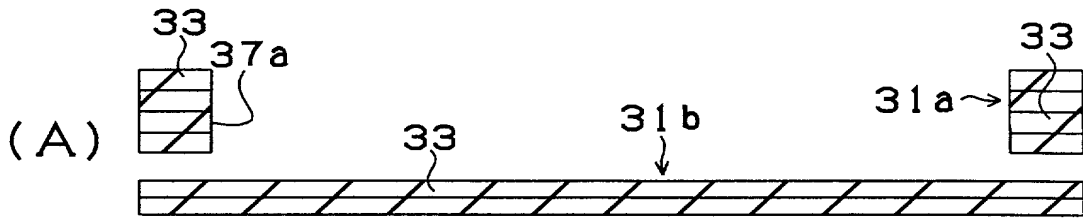
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Fig. 7

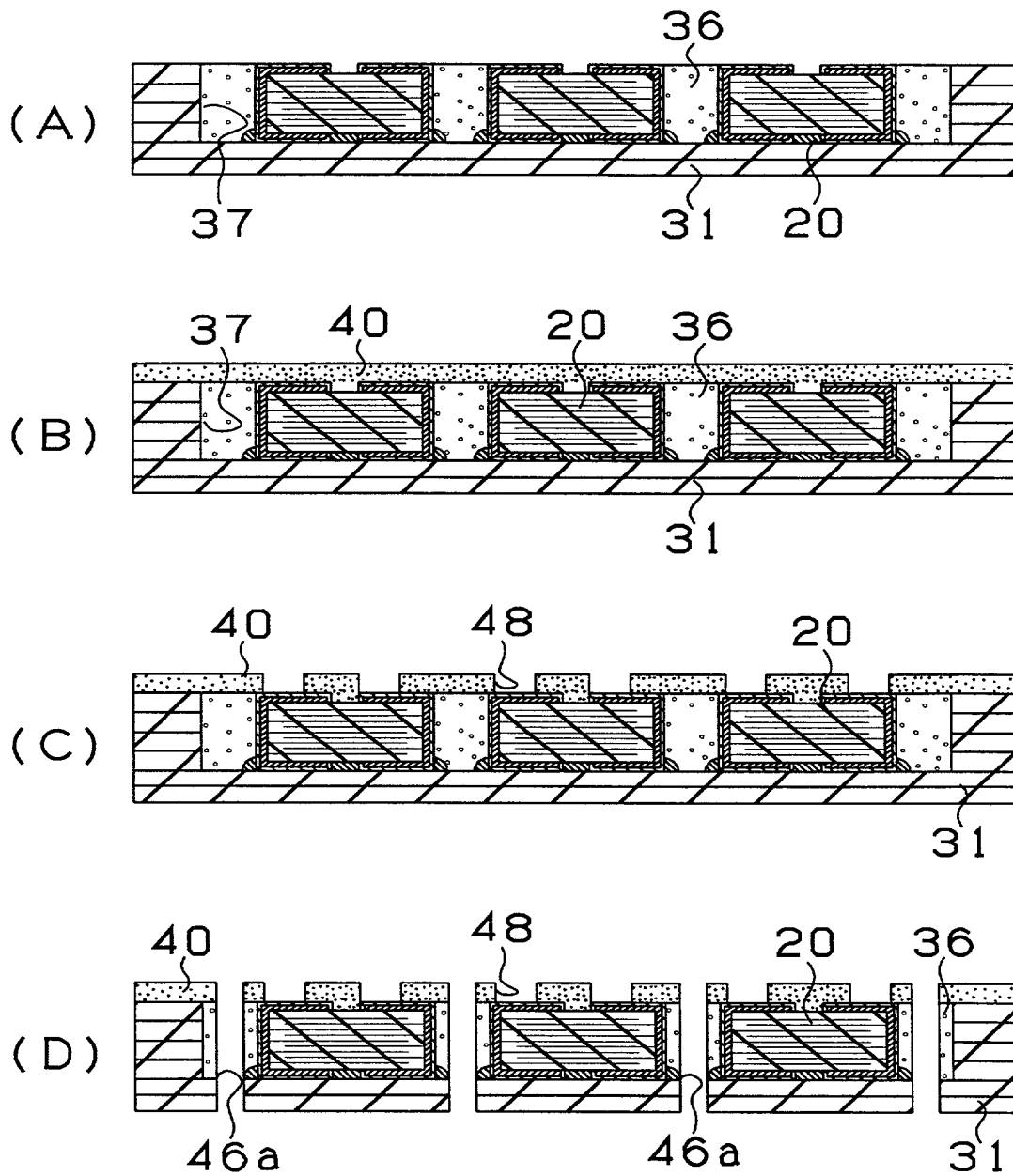


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Fig. 8

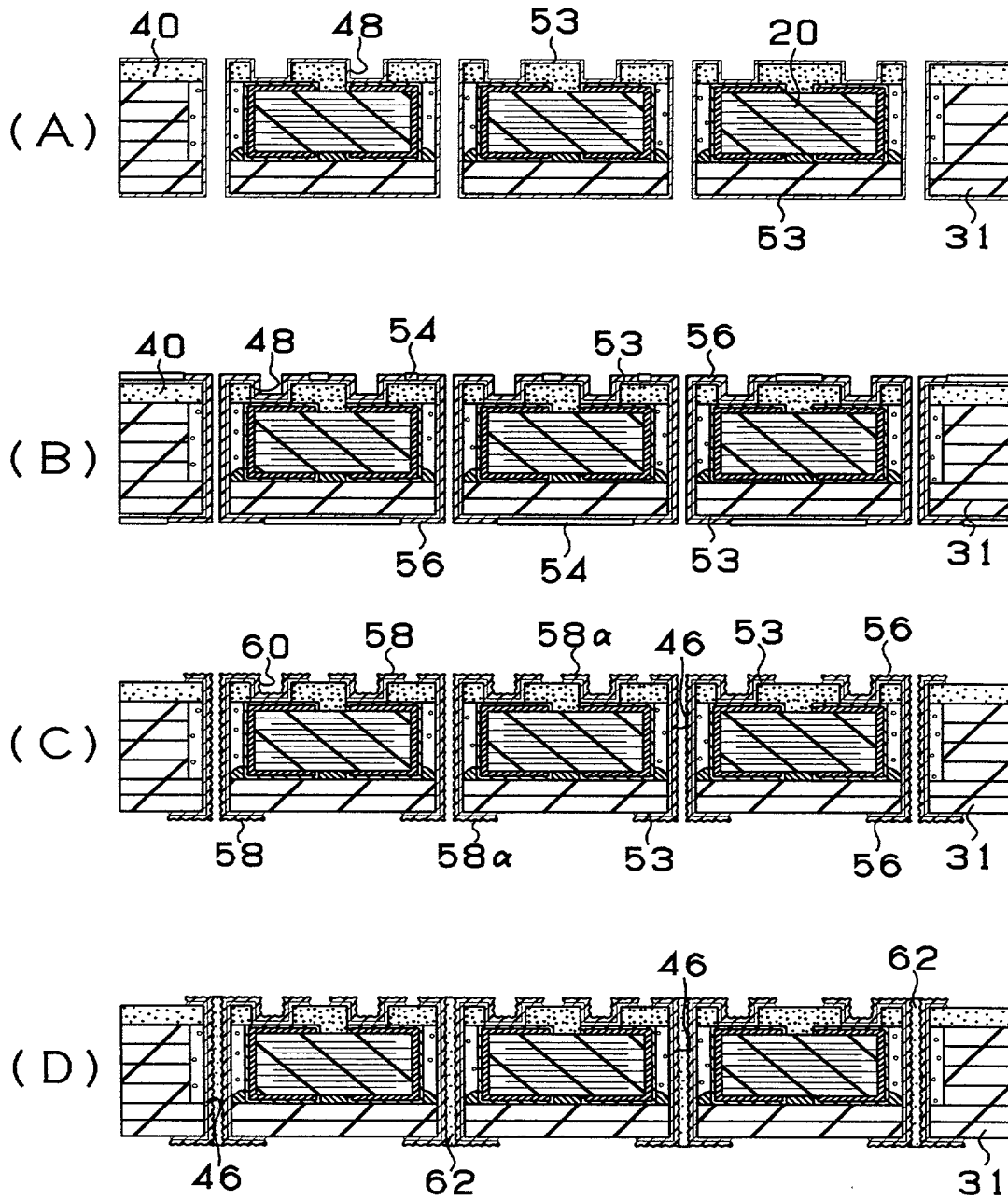


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Fig. 9

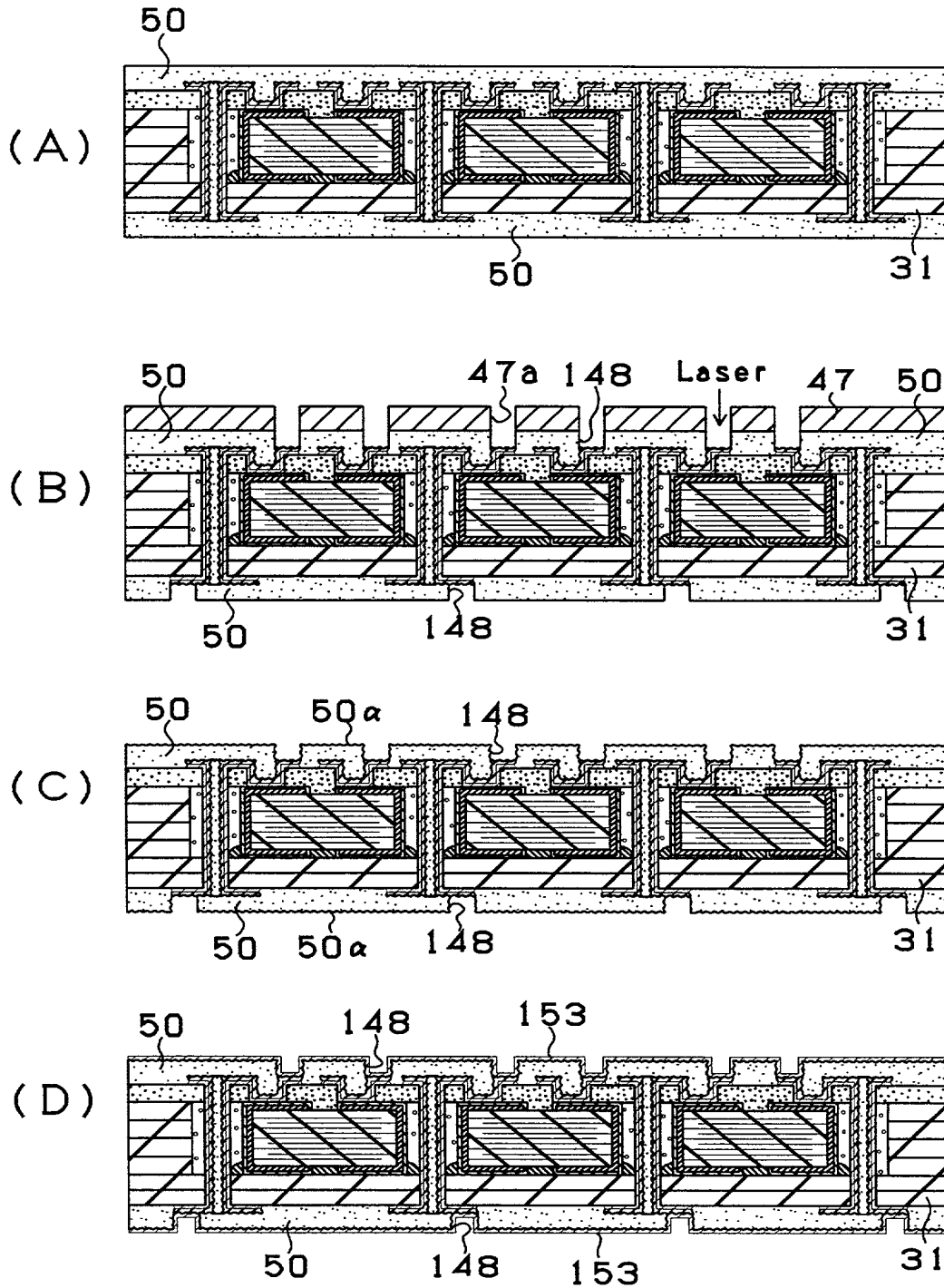


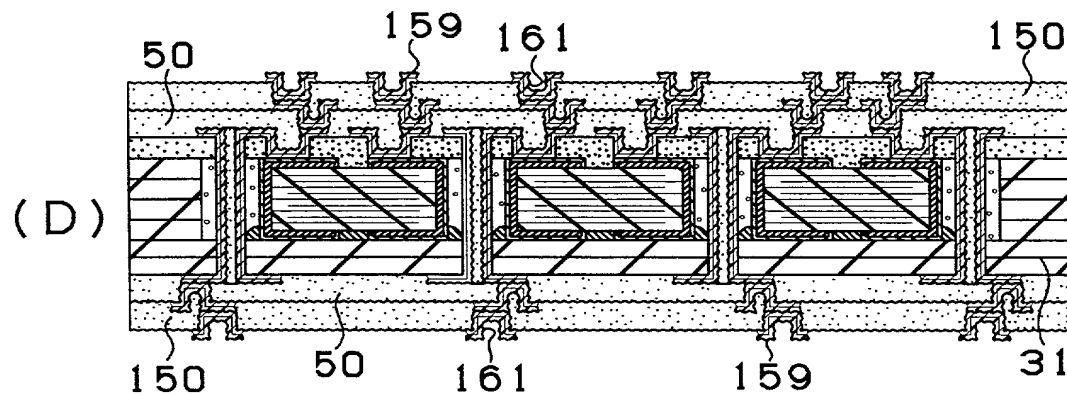
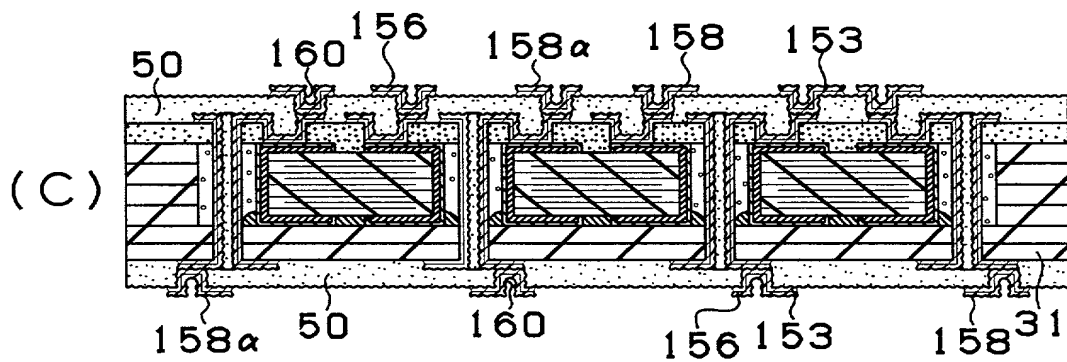
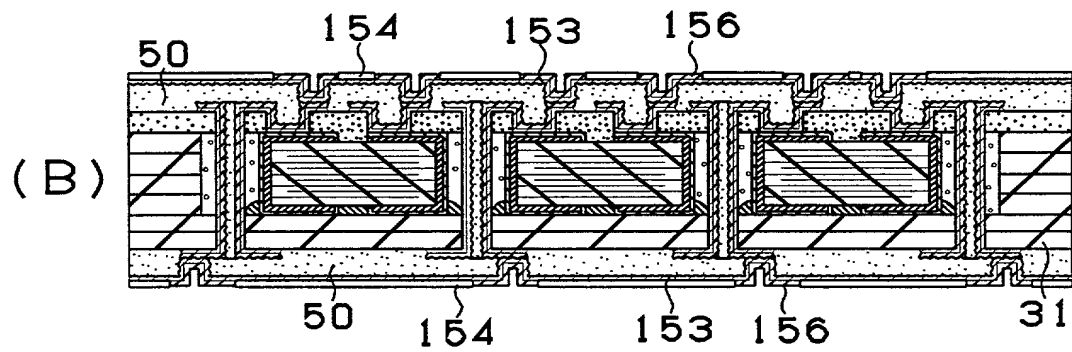
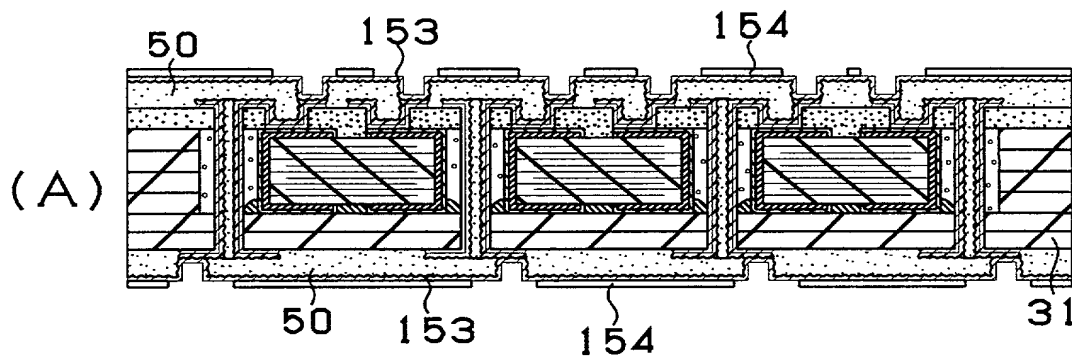
10/73
Fig. 10

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Fig. 11



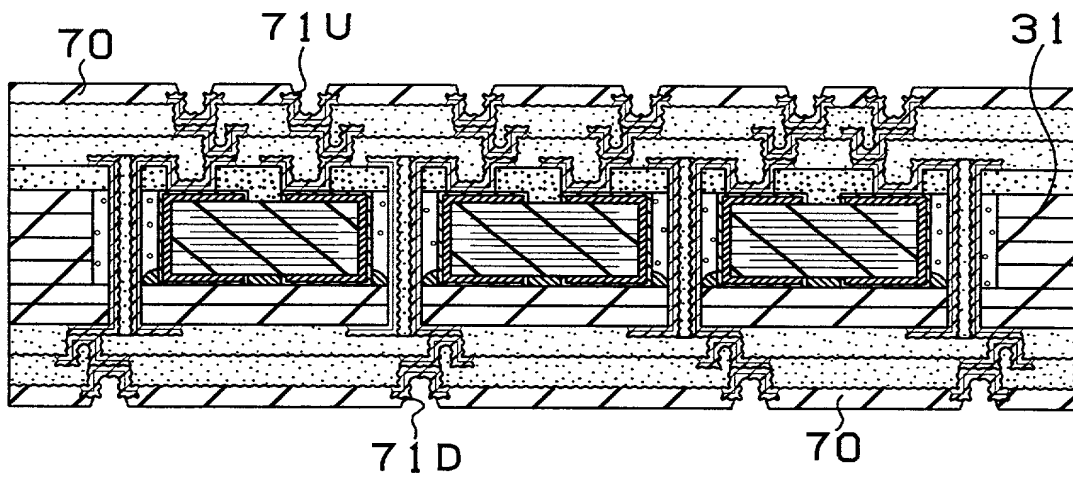
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Fig. 12



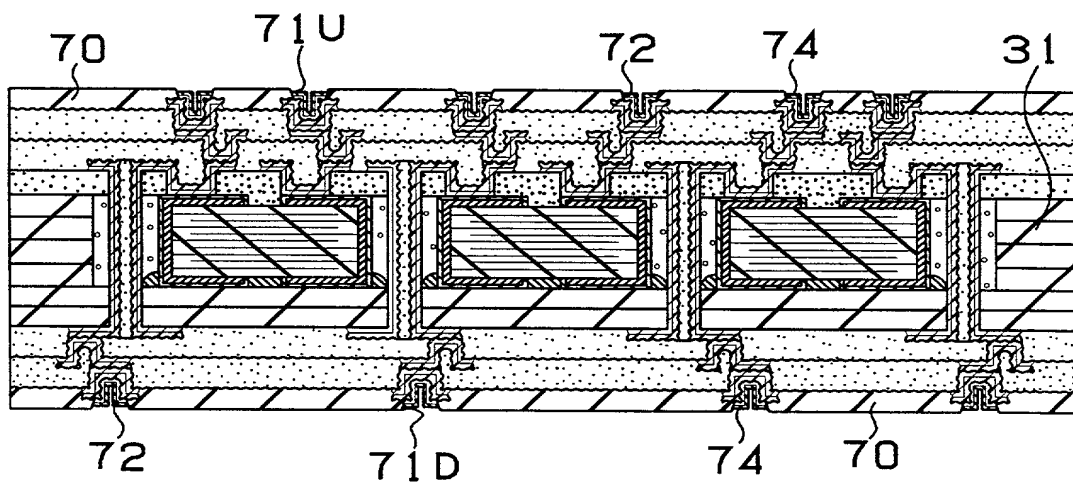
13/73
Fig. 13

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Fig. 14

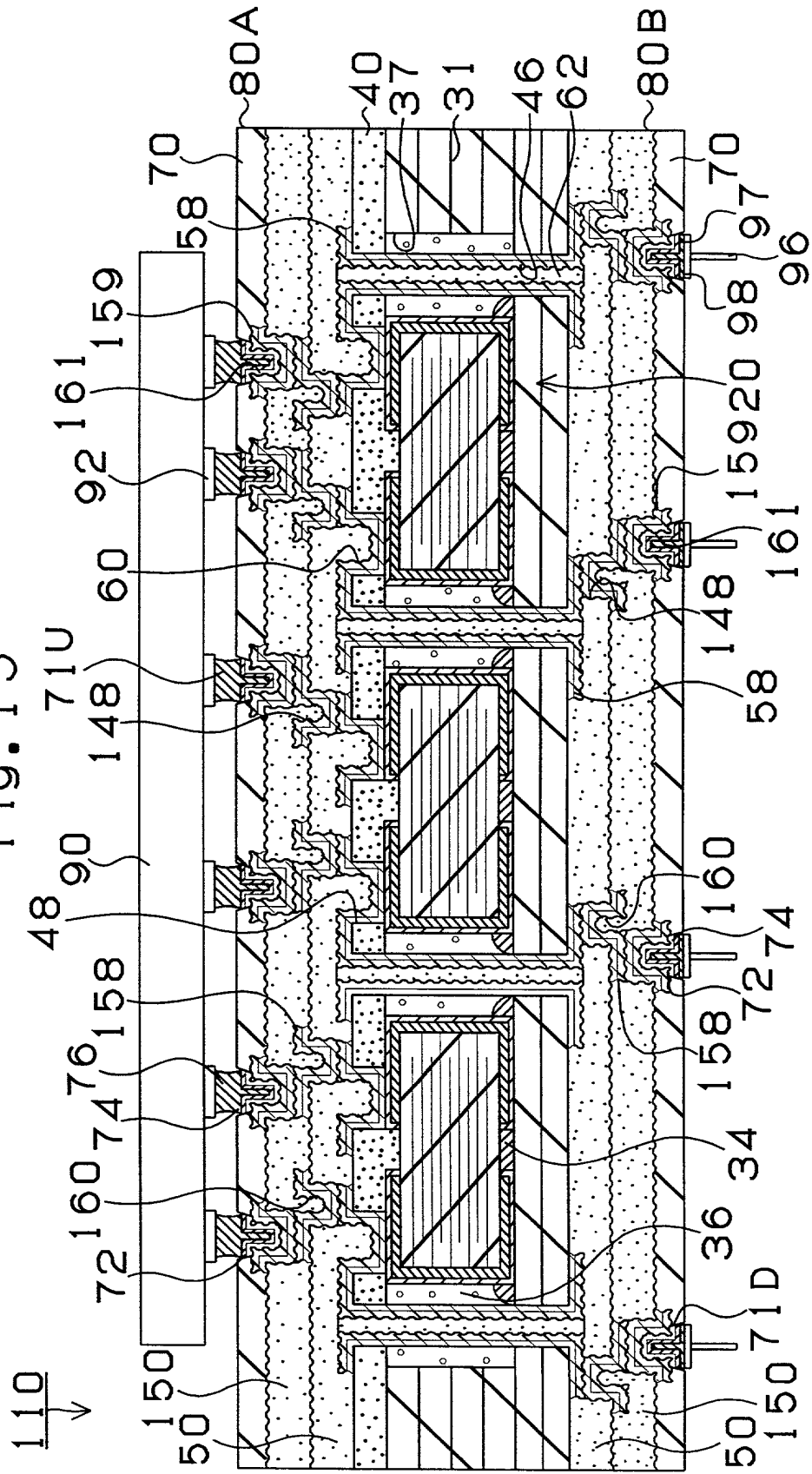
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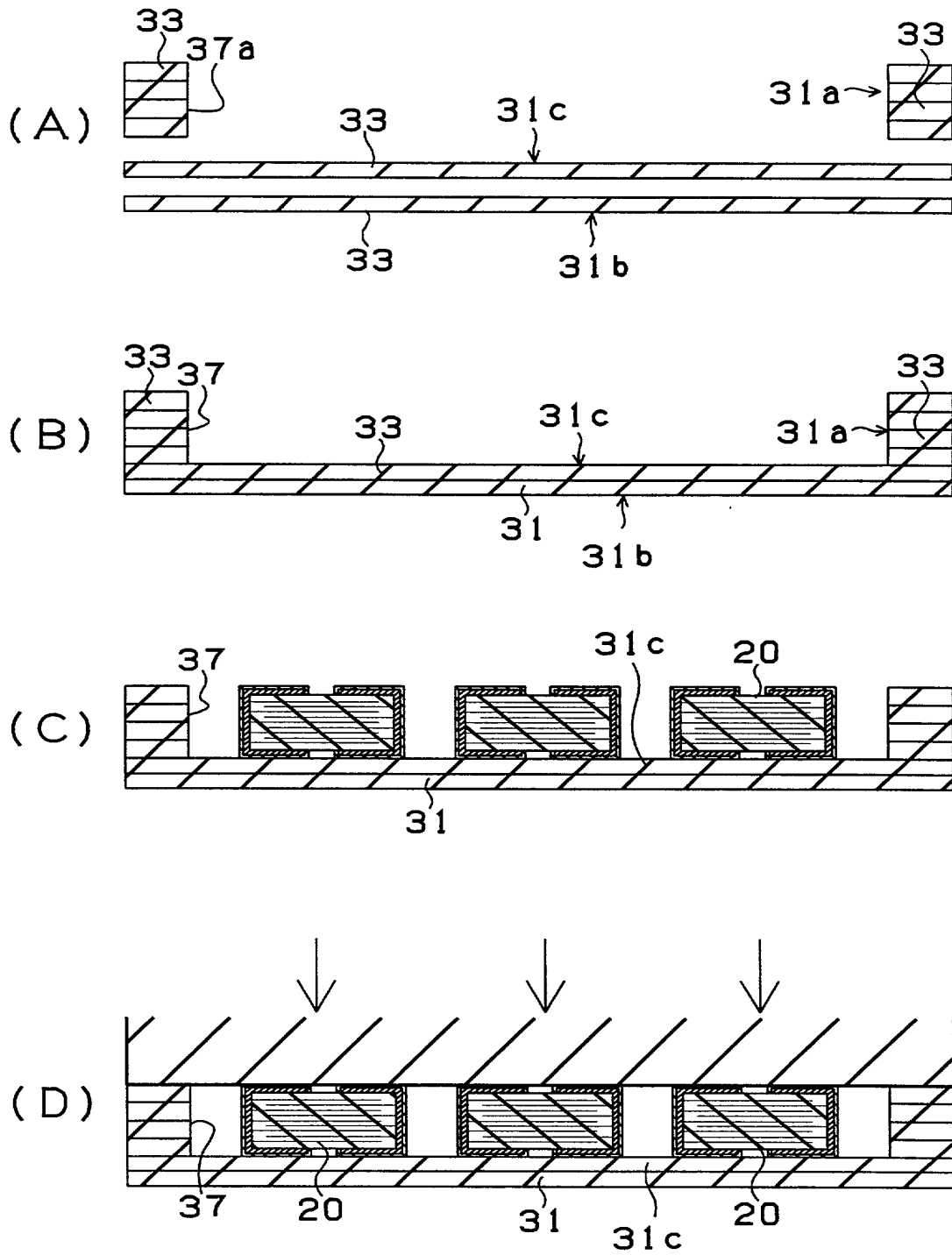


(B)



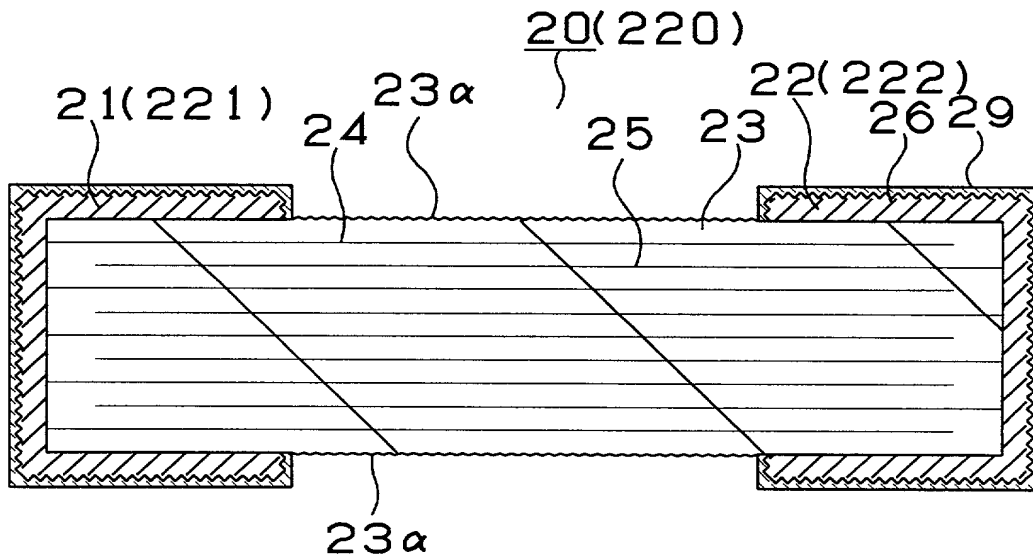
15/73
Fig. 15



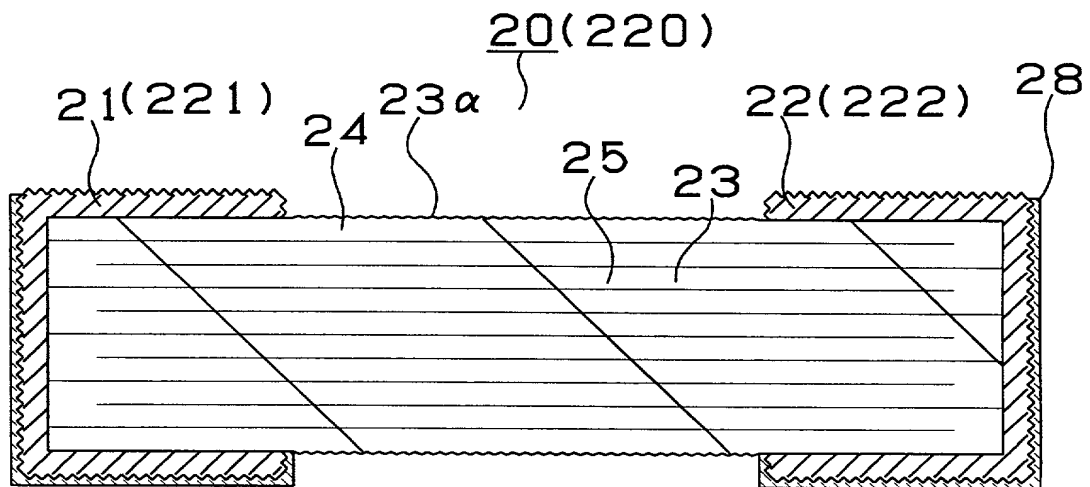
16/73
Fig. 16

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Fig. 17

(A)

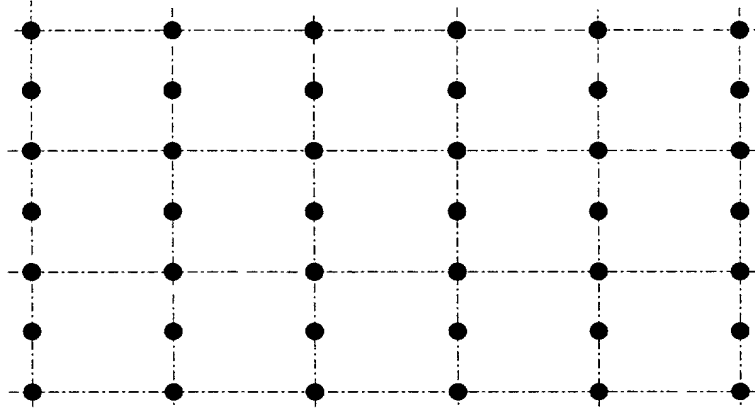


(B)

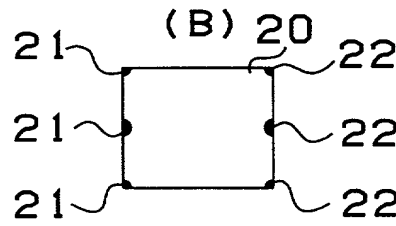


18/73
Fig. 18

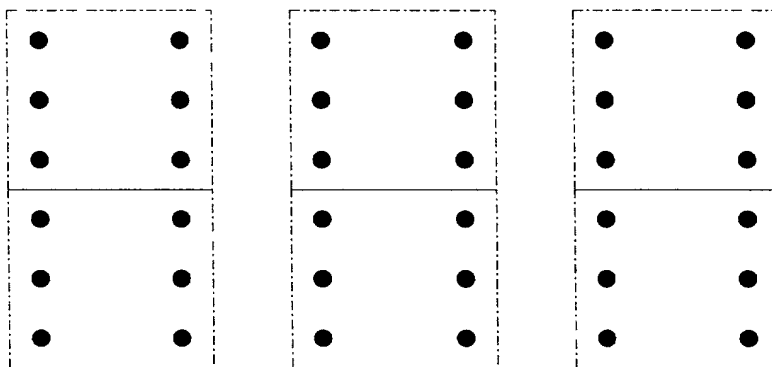
(A)



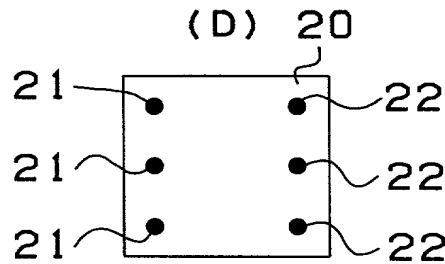
(B)



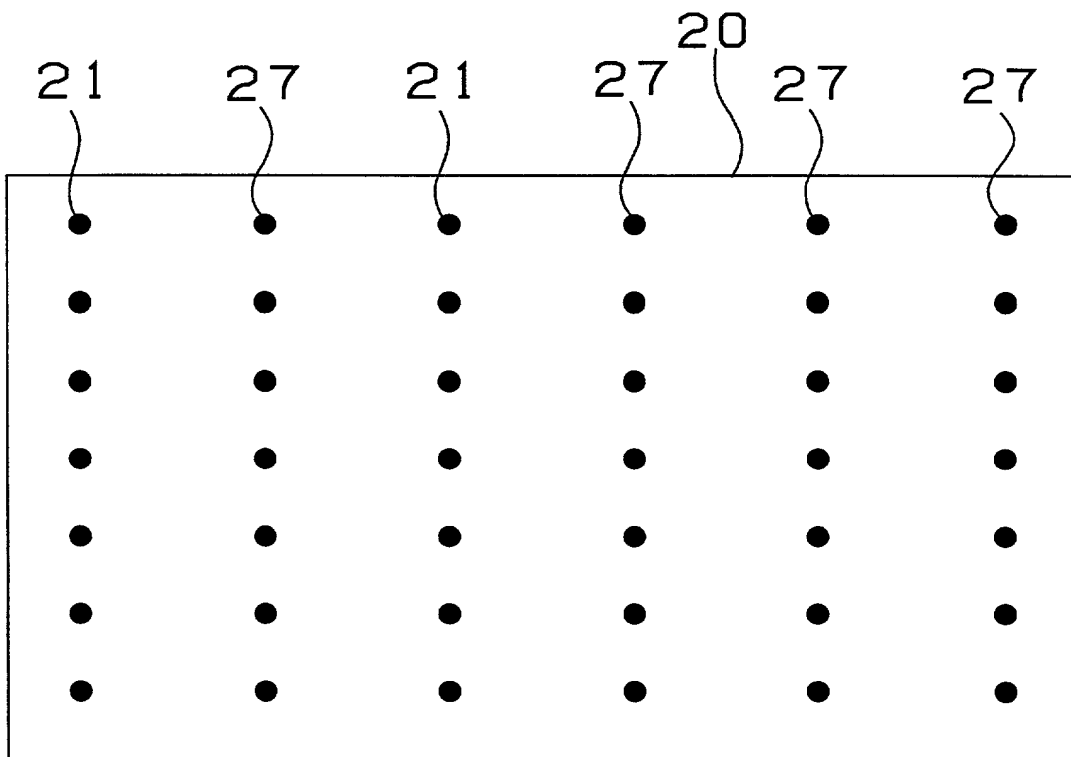
(C)



(D)

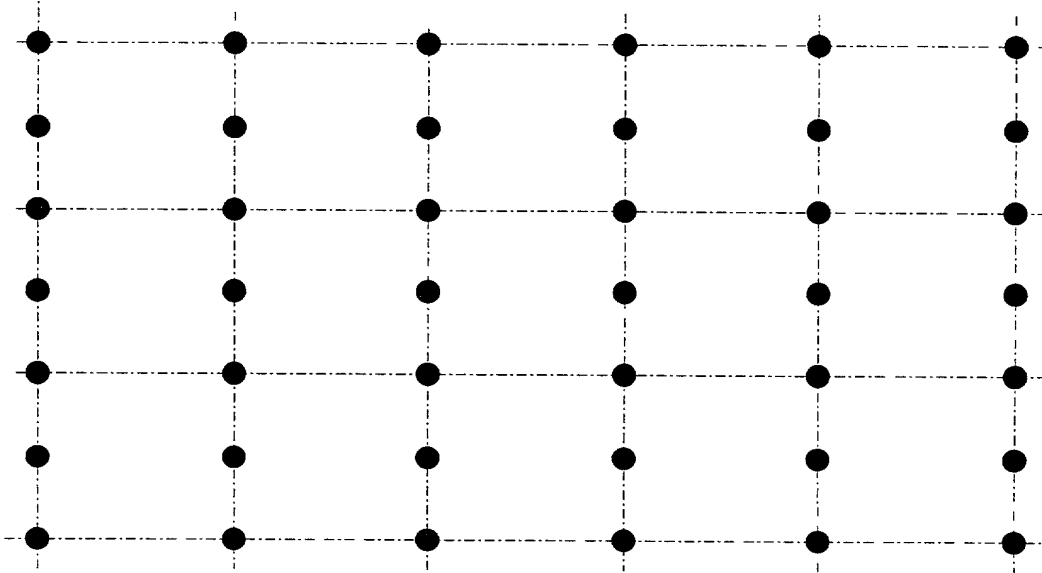


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Fig. 19



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Fig. 20

(A)



(B)

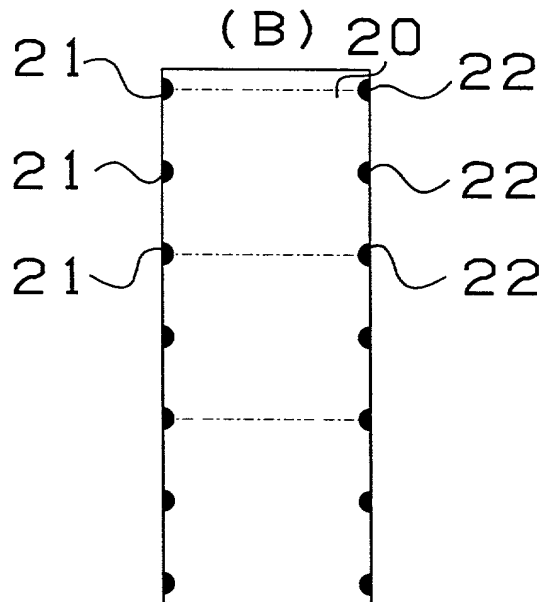
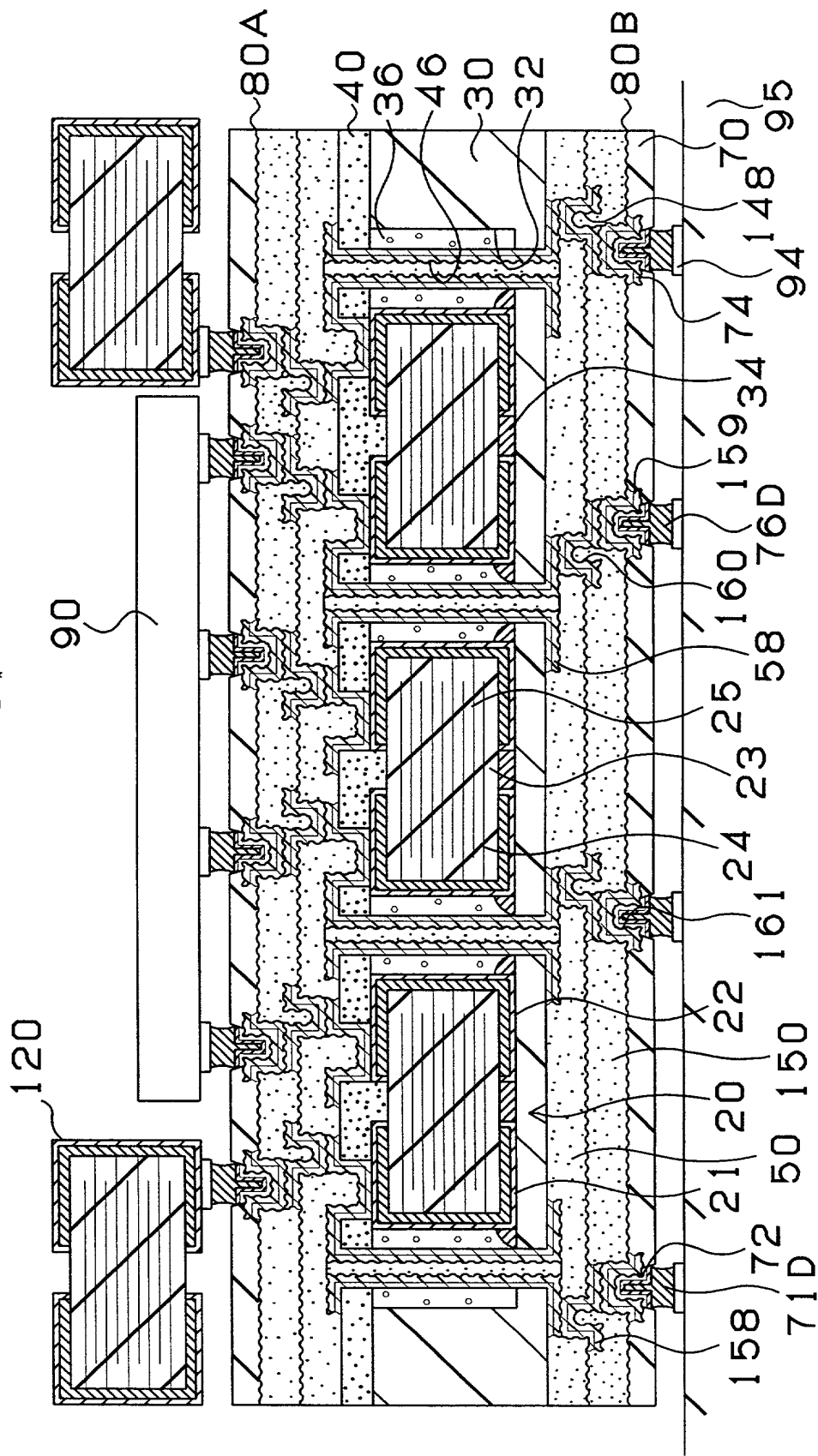


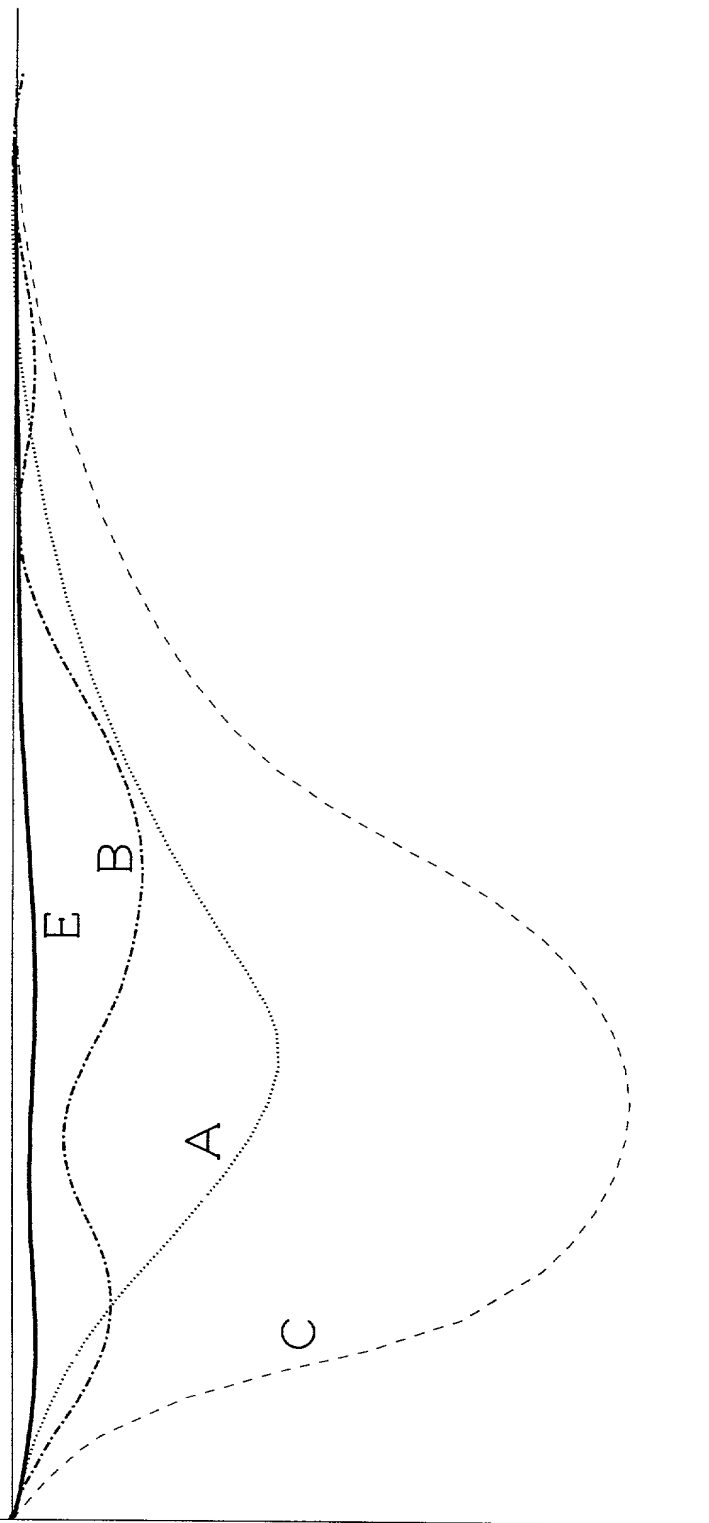
Fig. 21



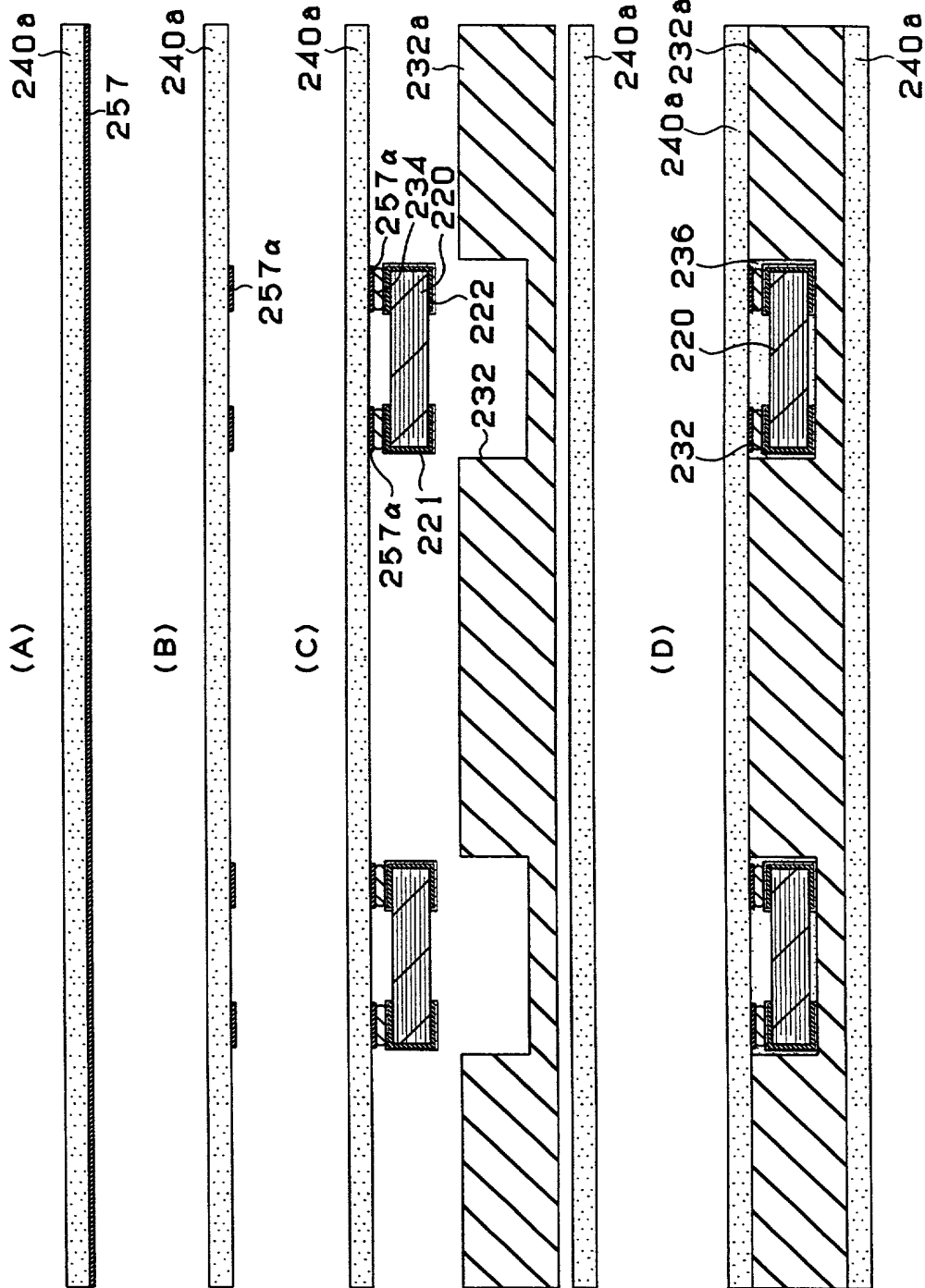
22/73
Fig. 22

Voltage

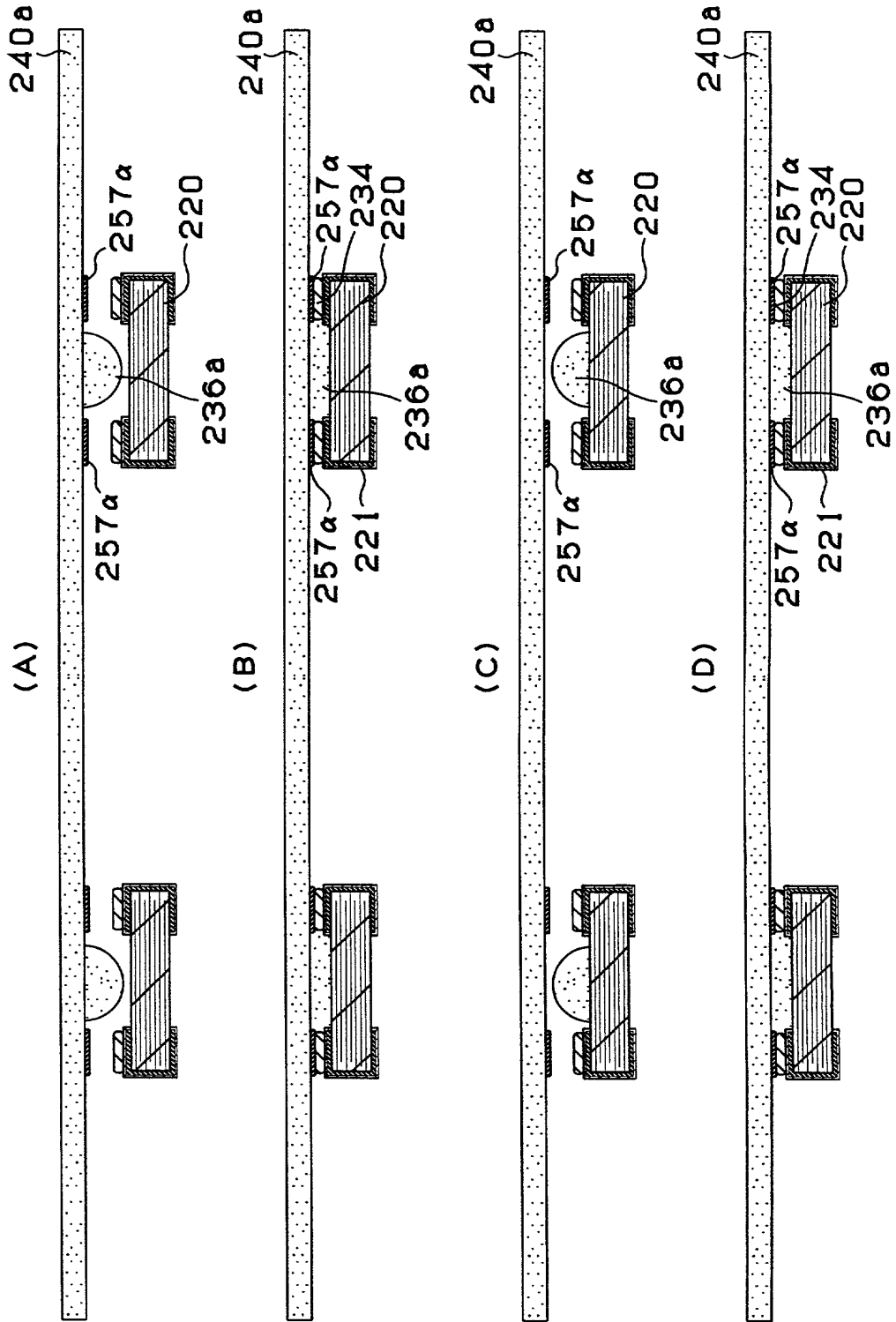
Time



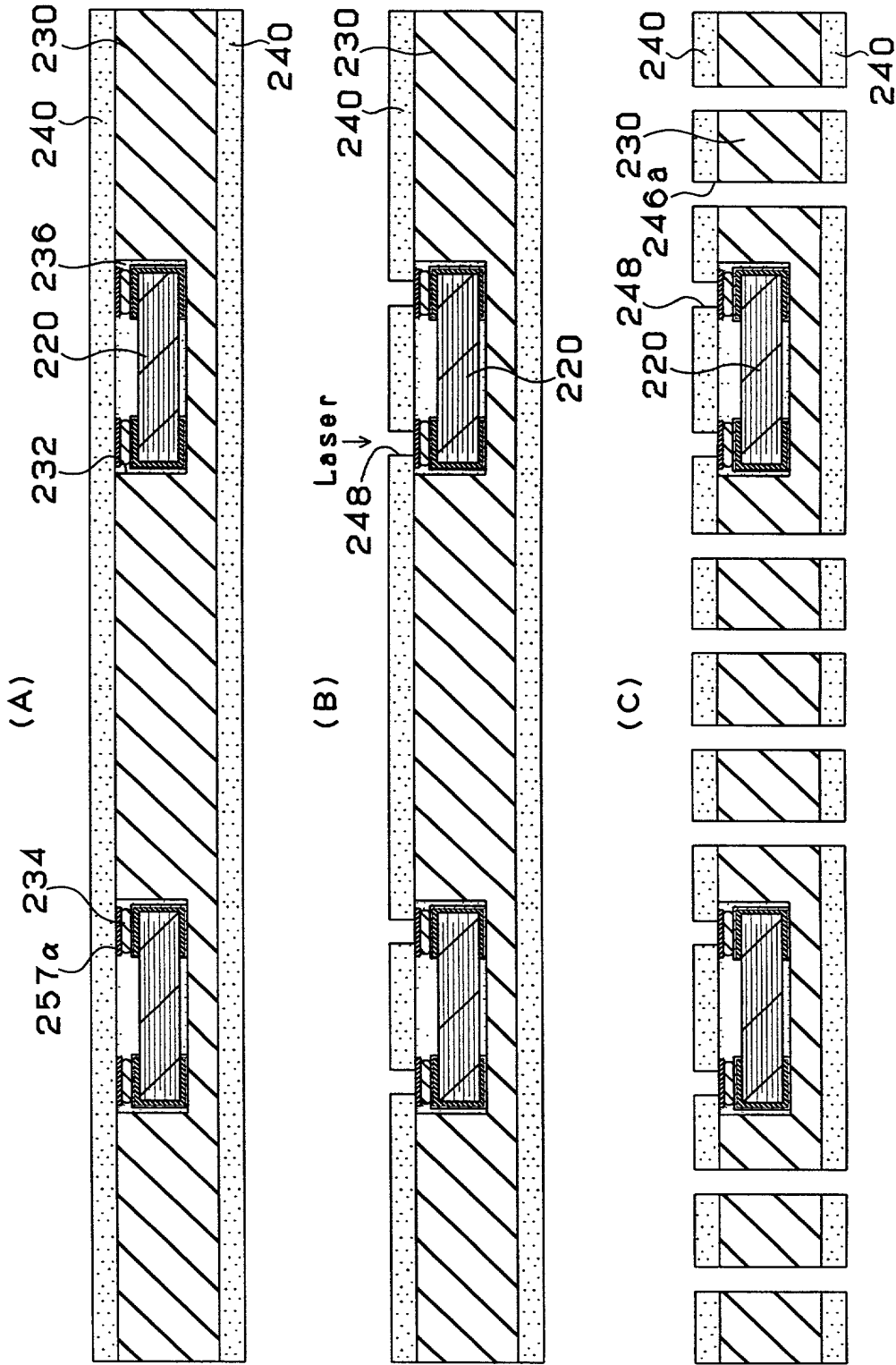
23/73
Fig. 23



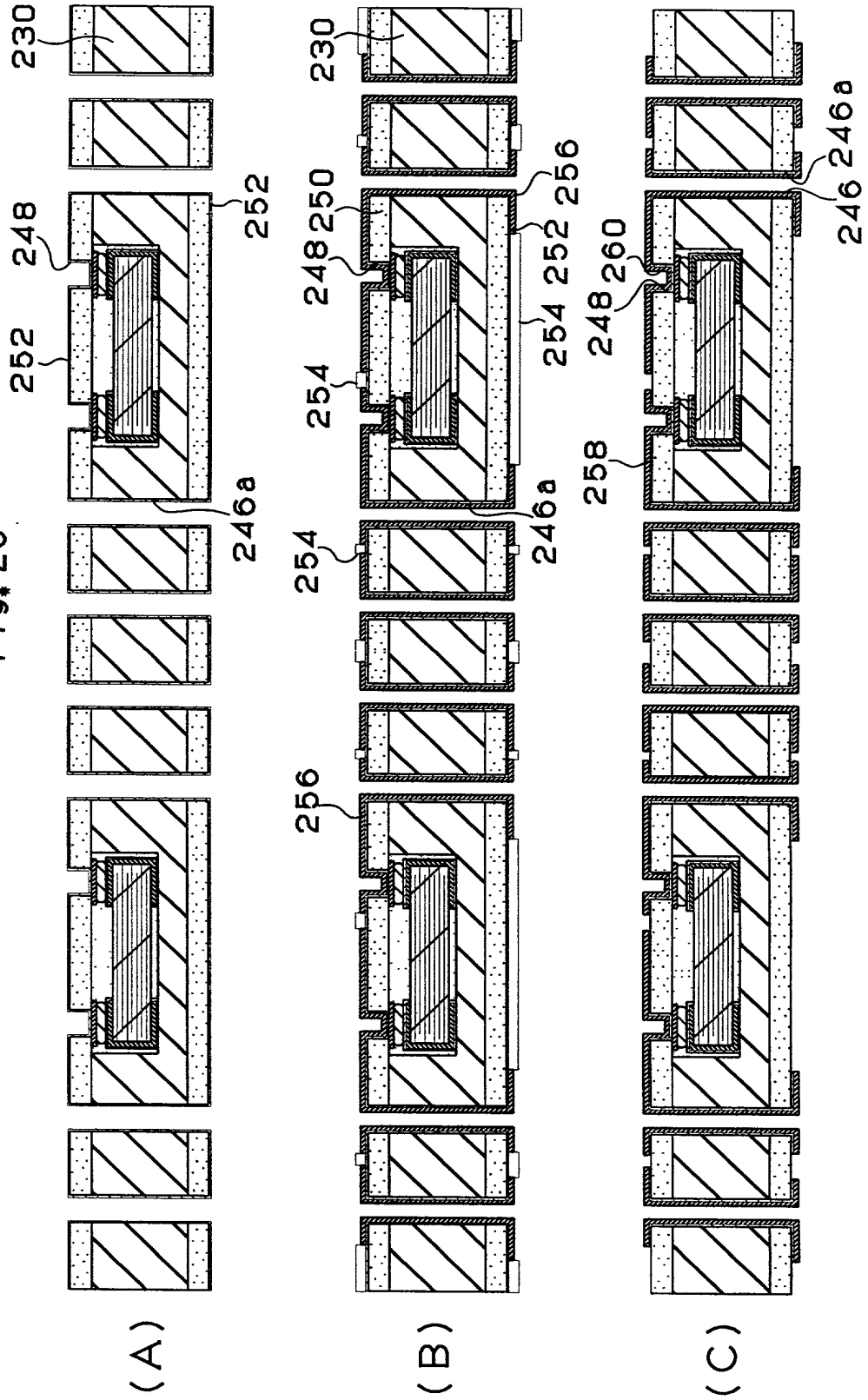
24/73
Fig. 24

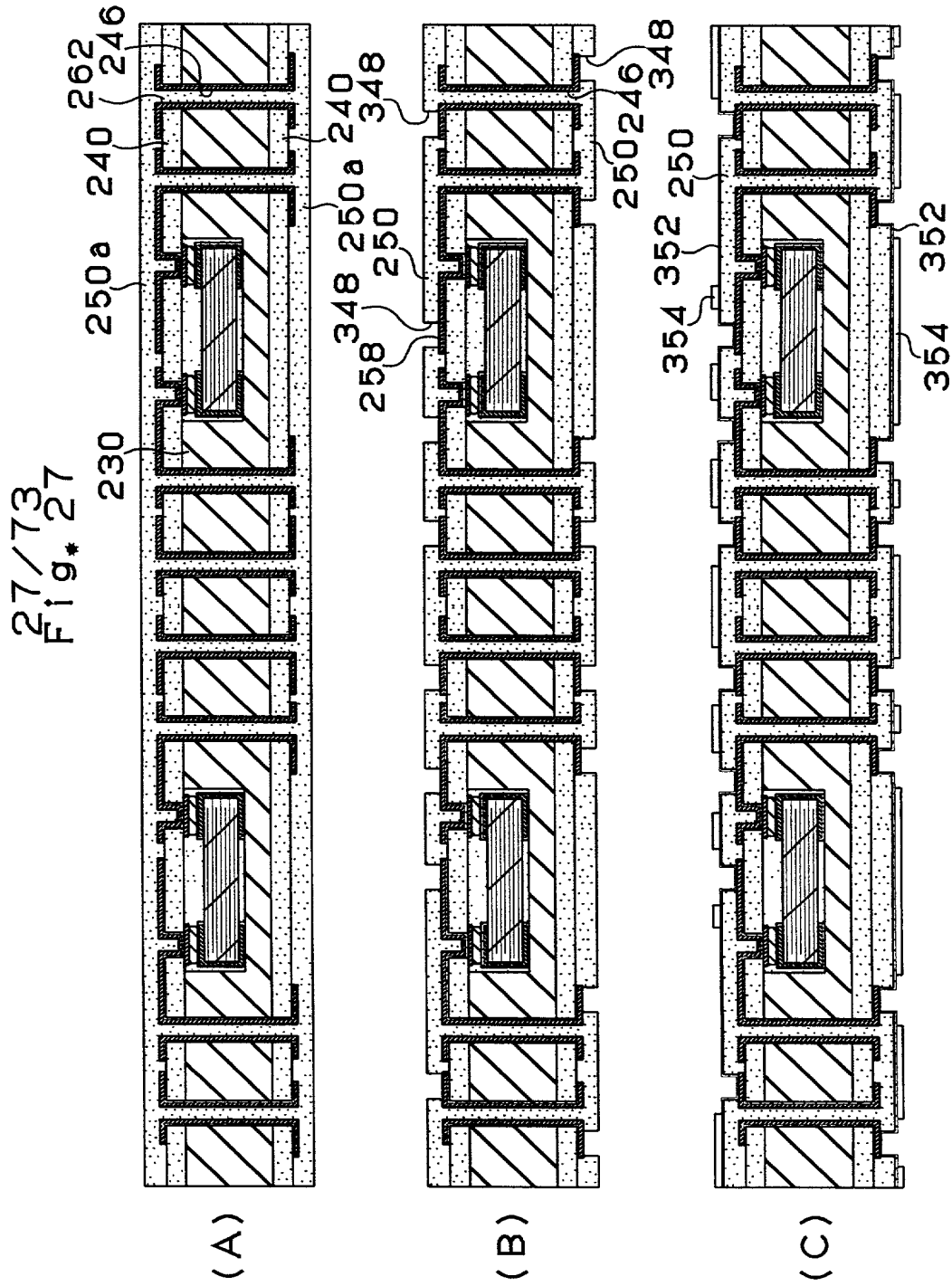


25/73
Fig. 25

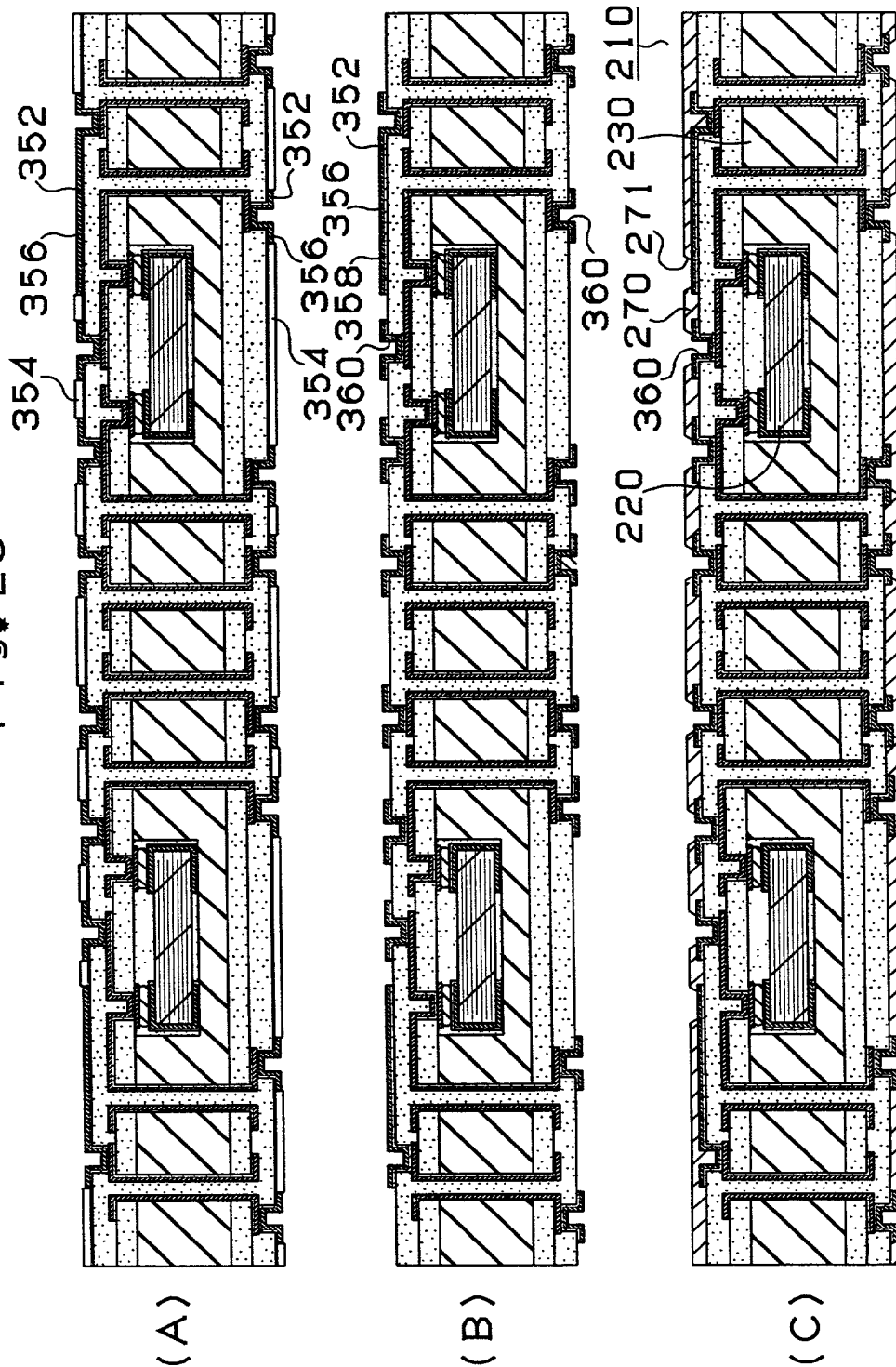


26/73
Fig. 26

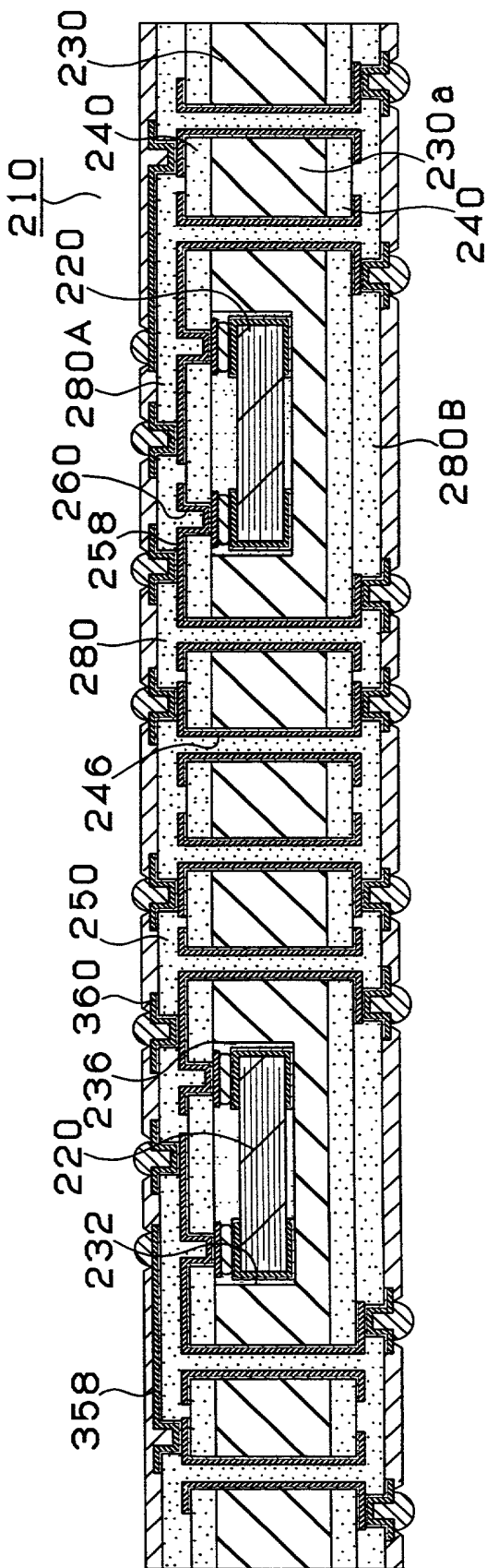




28/73
Fig. 28



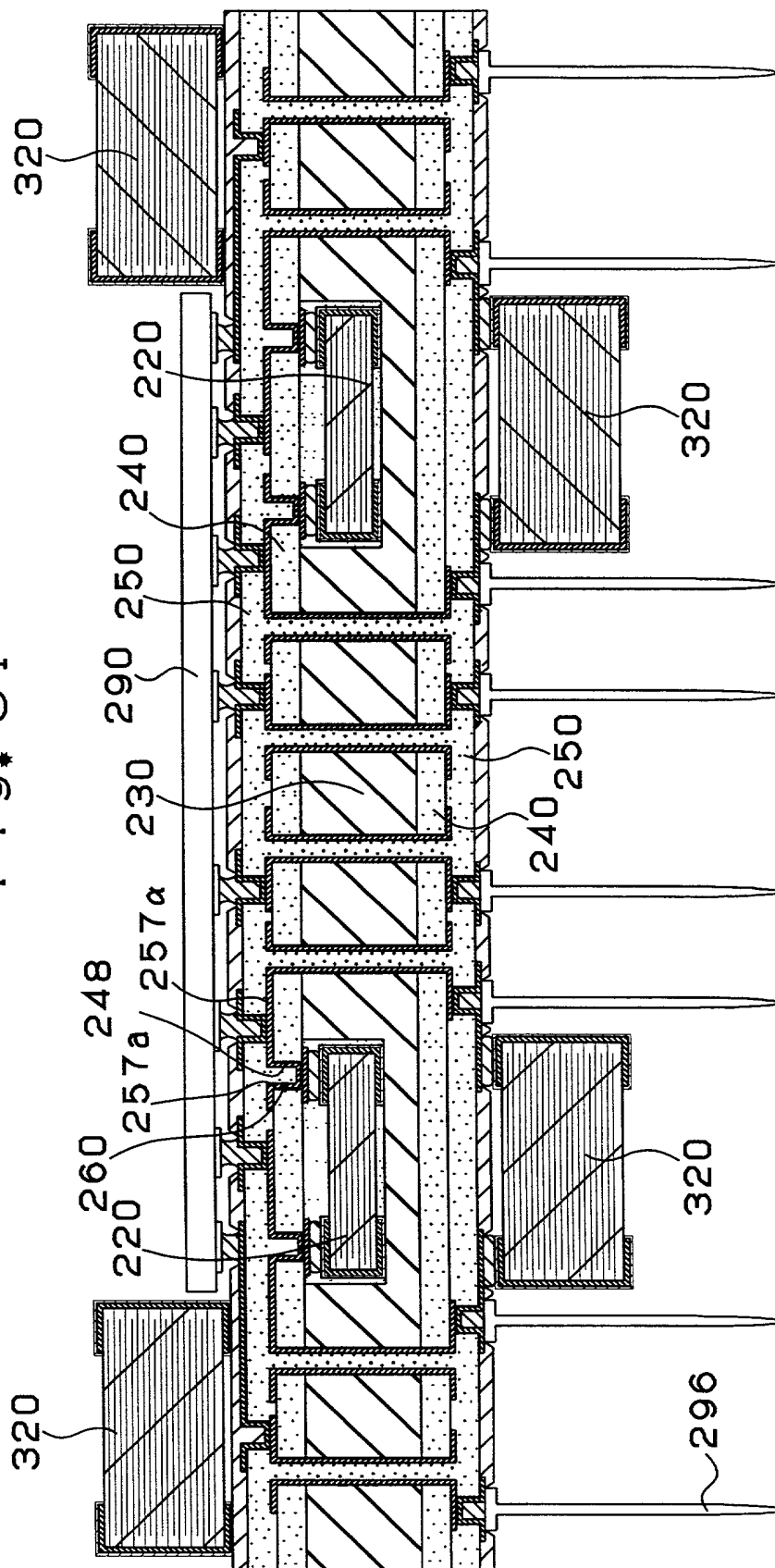
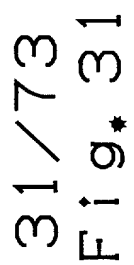
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Fig. 29



This cross-sectional diagram illustrates a complex multi-layered structure, likely a semiconductor device or a specialized substrate. The structure consists of several alternating layers of different materials, represented by various hatching patterns (diagonal lines, dots, horizontal lines, etc.). Key components include:

- Top Layer (210):** A thin layer at the very top.
- Substrate Layers (220, 221, 222, 223, 224, 225):** Multiple layers forming the base of the device.
- Conductive Layers (230, 231, 232, 233, 234, 235):** Layers containing conductive material, possibly copper or aluminum, used for interconnects.
- Dielectric Layers (240, 241, 242, 243, 244, 245):** Insulating layers separating the conductive layers.
- Passivation Layer (250):** A protective layer on the bottom surface.
- Interconnect Pads (260, 270, 280, 290):** Specific regions designed for electrical connections.
- Through-Holes/Vias (211, 212, 213, 214, 215):** Vertical openings connecting different layers.

The diagram shows a highly integrated design with precise alignment between the various functional layers.



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Fig. 32

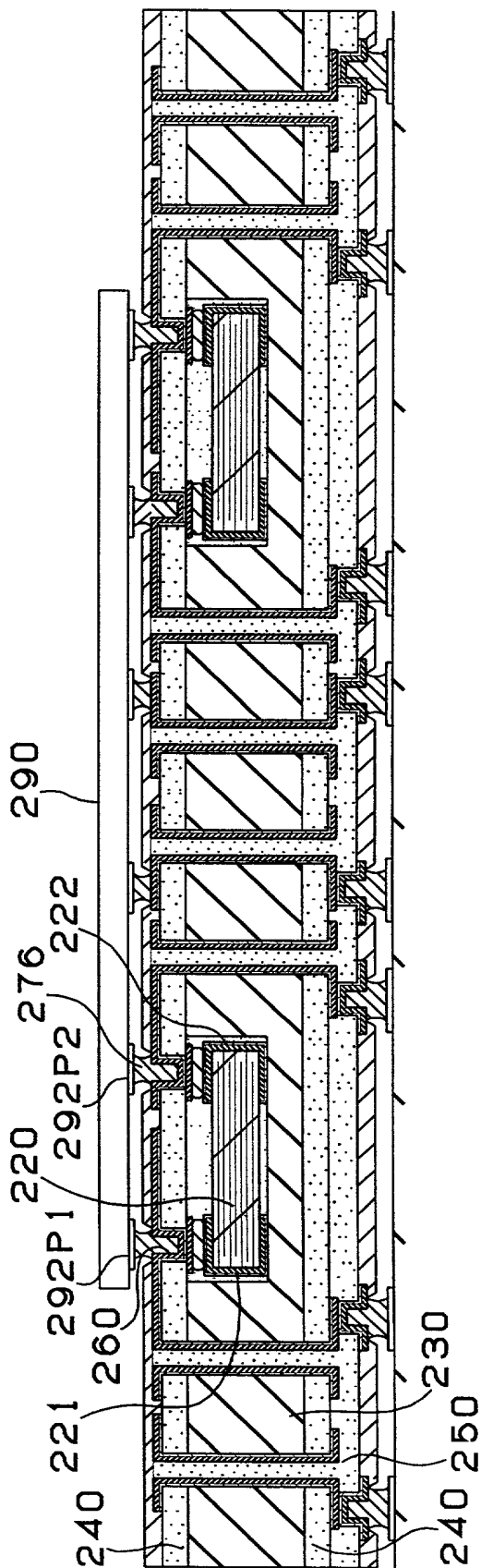


Fig. 33/733

3. 9. 1950

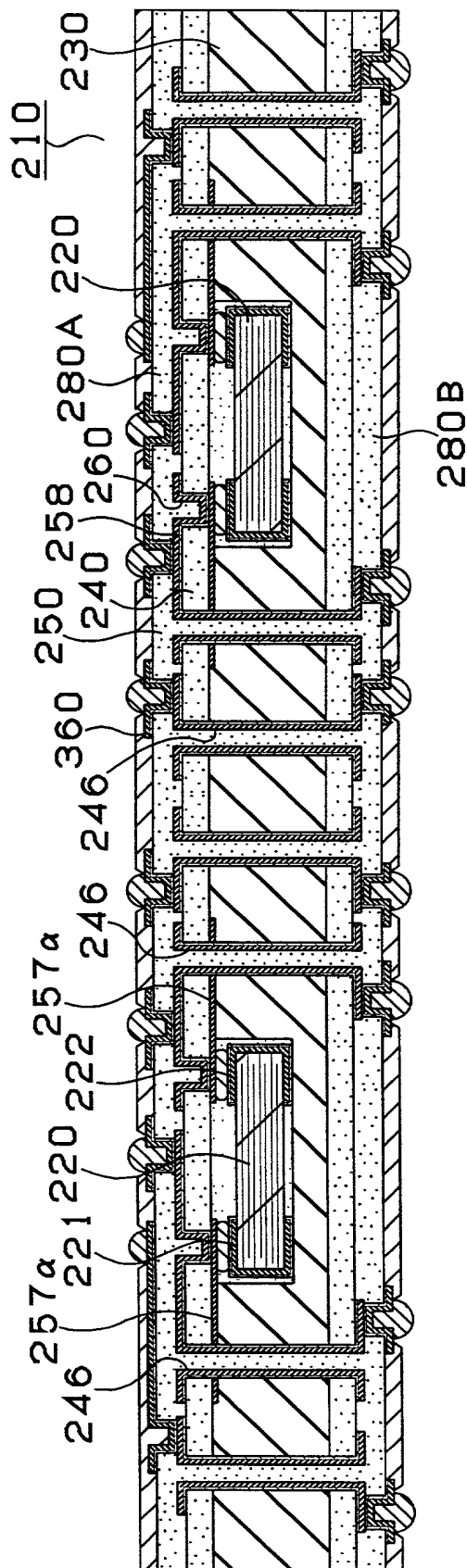


Figure 6 shows four cross-sectional views of semiconductor devices labeled (A), (B), (C), and (D).
 (A) Shows a substrate with a top layer 435 and two patterned regions 432a and 432b.
 (B) Shows a substrate with a top layer 430a and a central patterned region 420. The region 420 has a core 428 and is surrounded by layers 421, 422, 436a, and 437. The entire structure is flanked by regions 432a and 432b.
 (C) Shows a substrate with a top layer 430a and a central patterned region 420. The region 420 has a core 428 and is surrounded by layers 436 and 437. The entire structure is flanked by regions 432a and 432b.
 (D) Shows a substrate with a top layer 440 and a central patterned region 420. The region 420 has a core 428 and is surrounded by layers 436 and 437. The entire structure is flanked by regions 432a and 432b.

35/73
Fig. 35

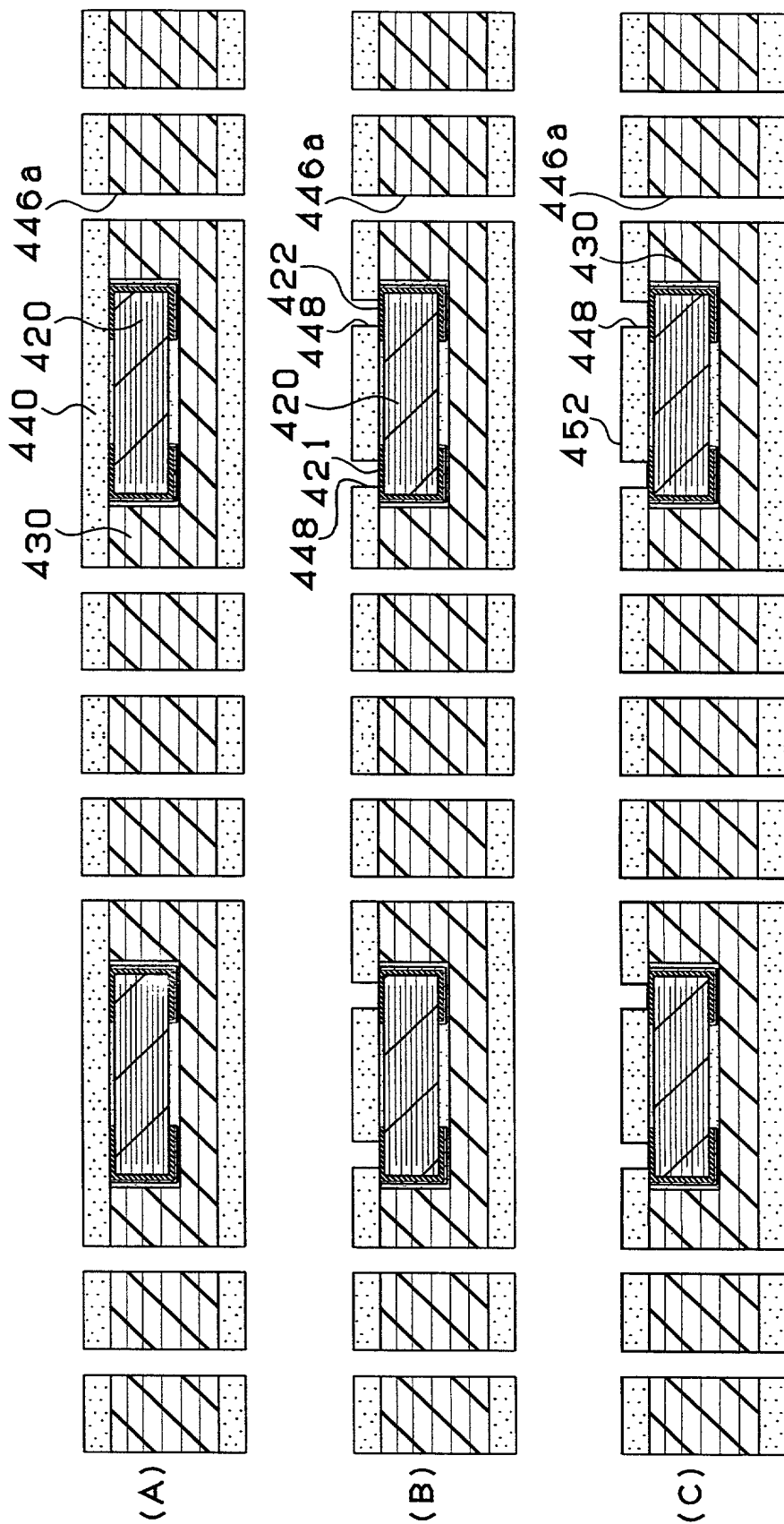
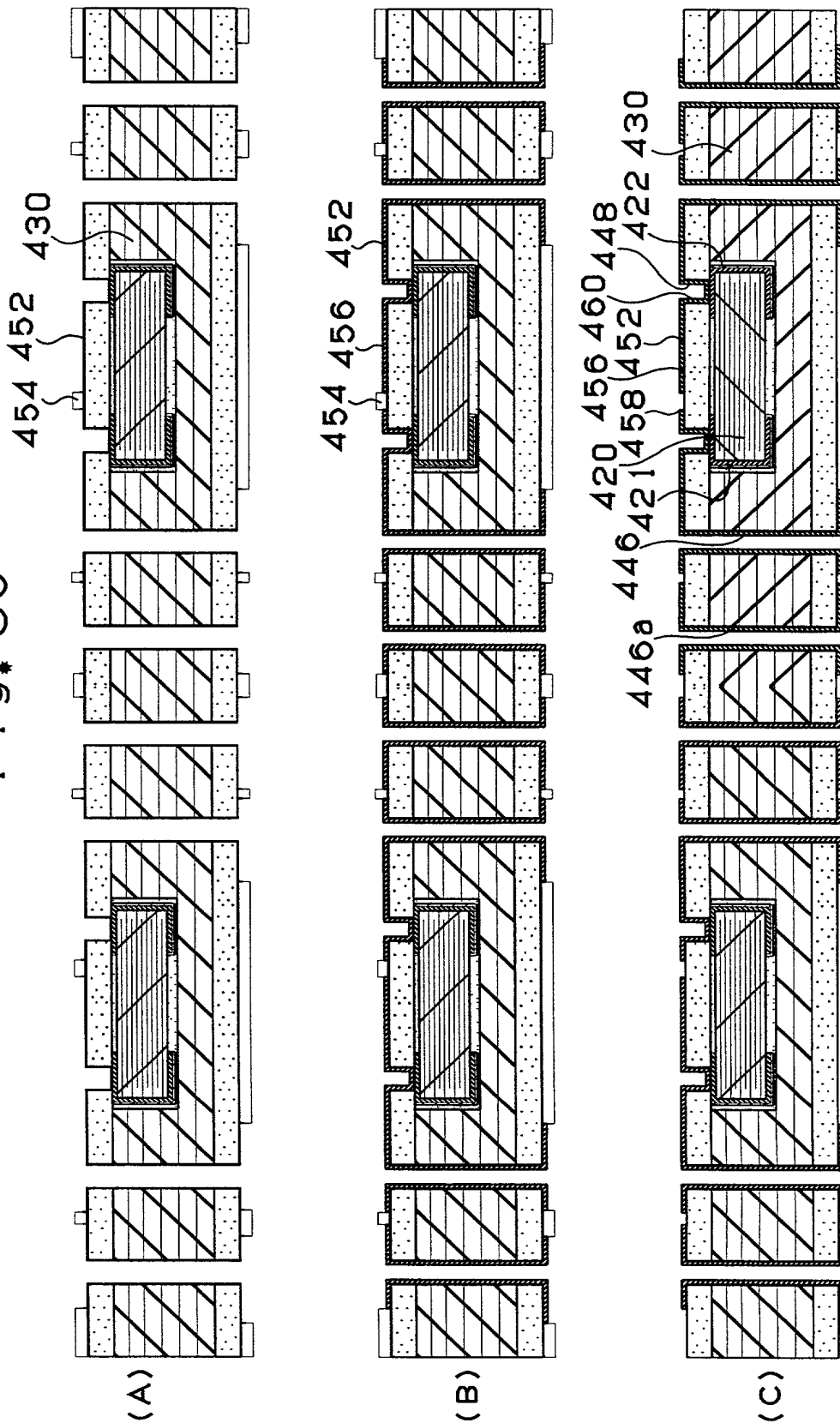
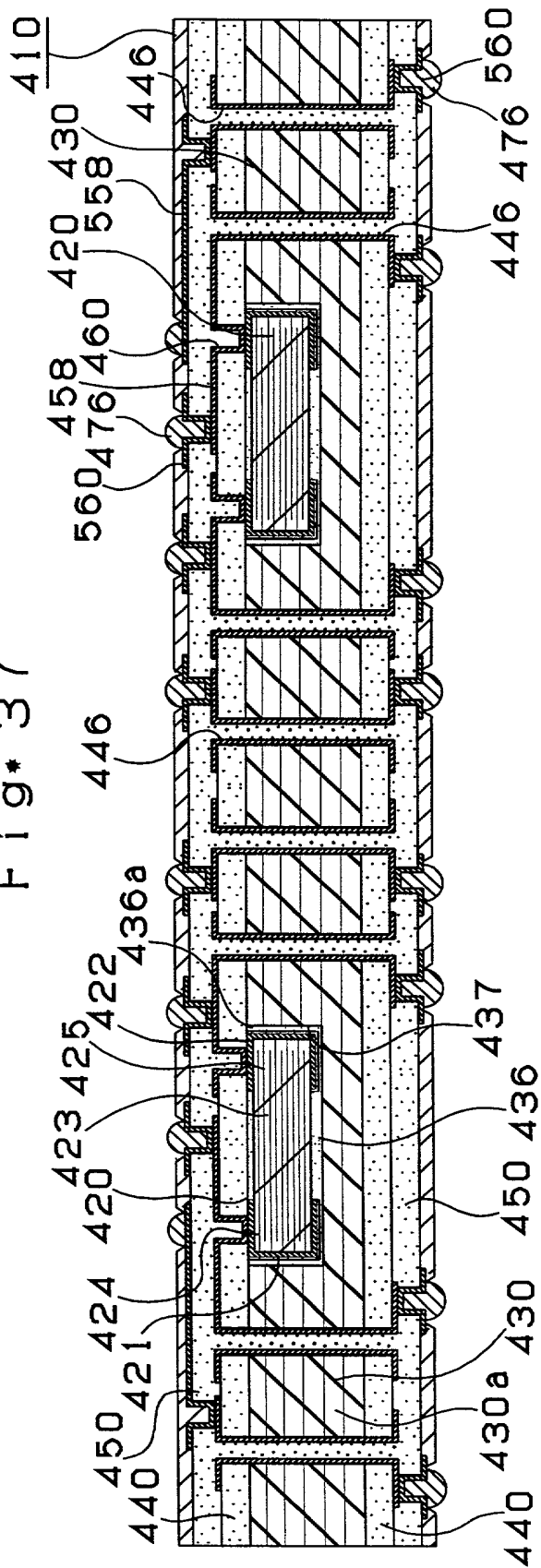


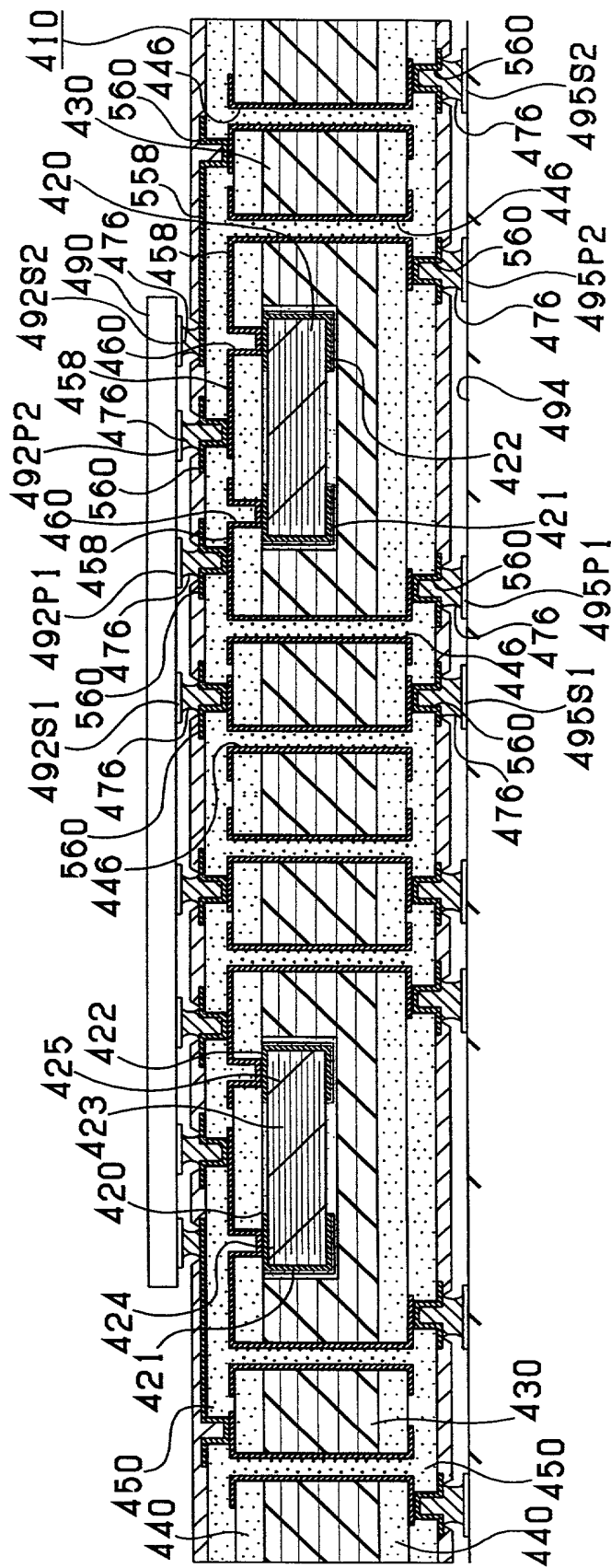
Fig. 36



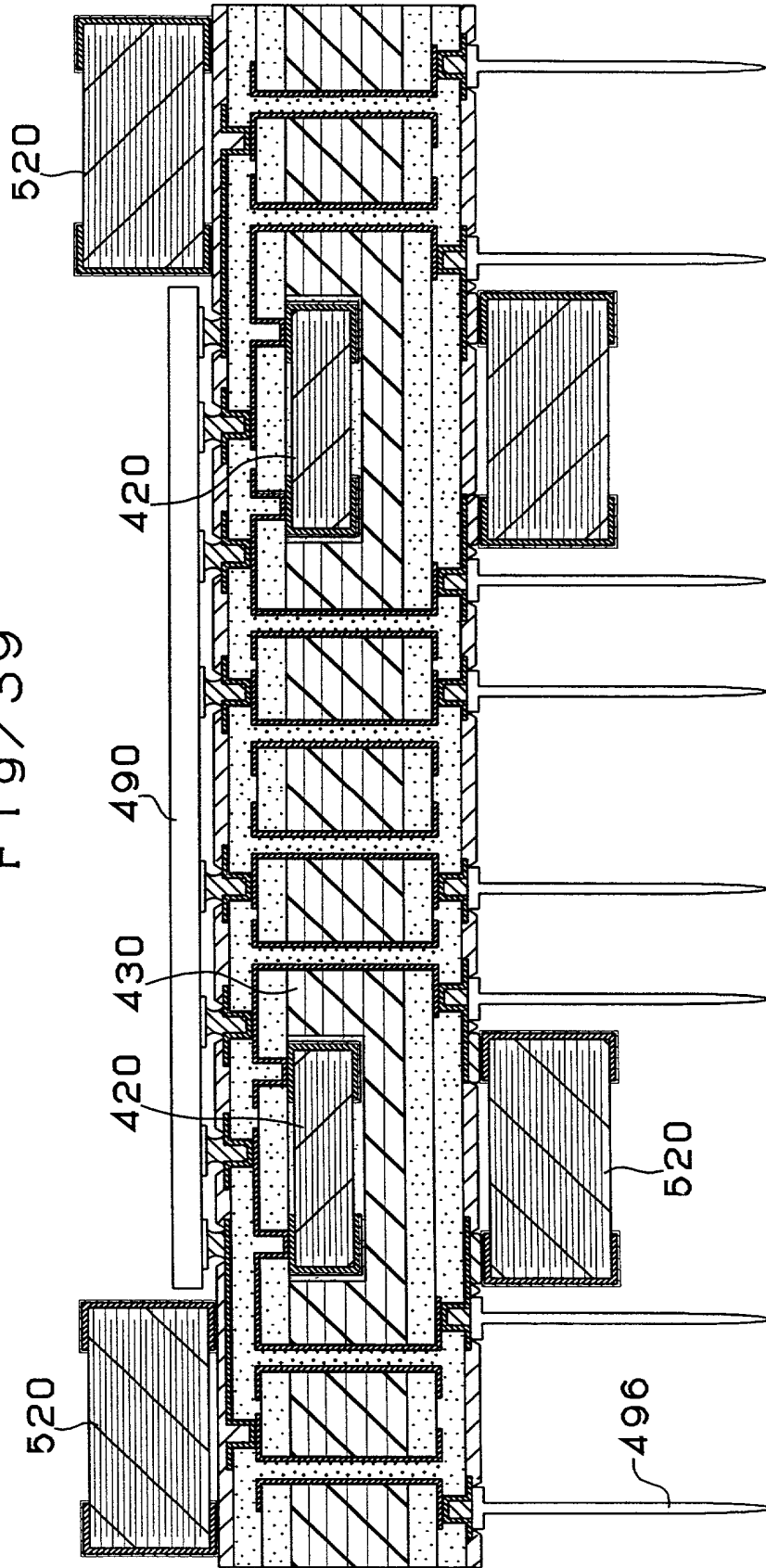
37/73
Fig* 37



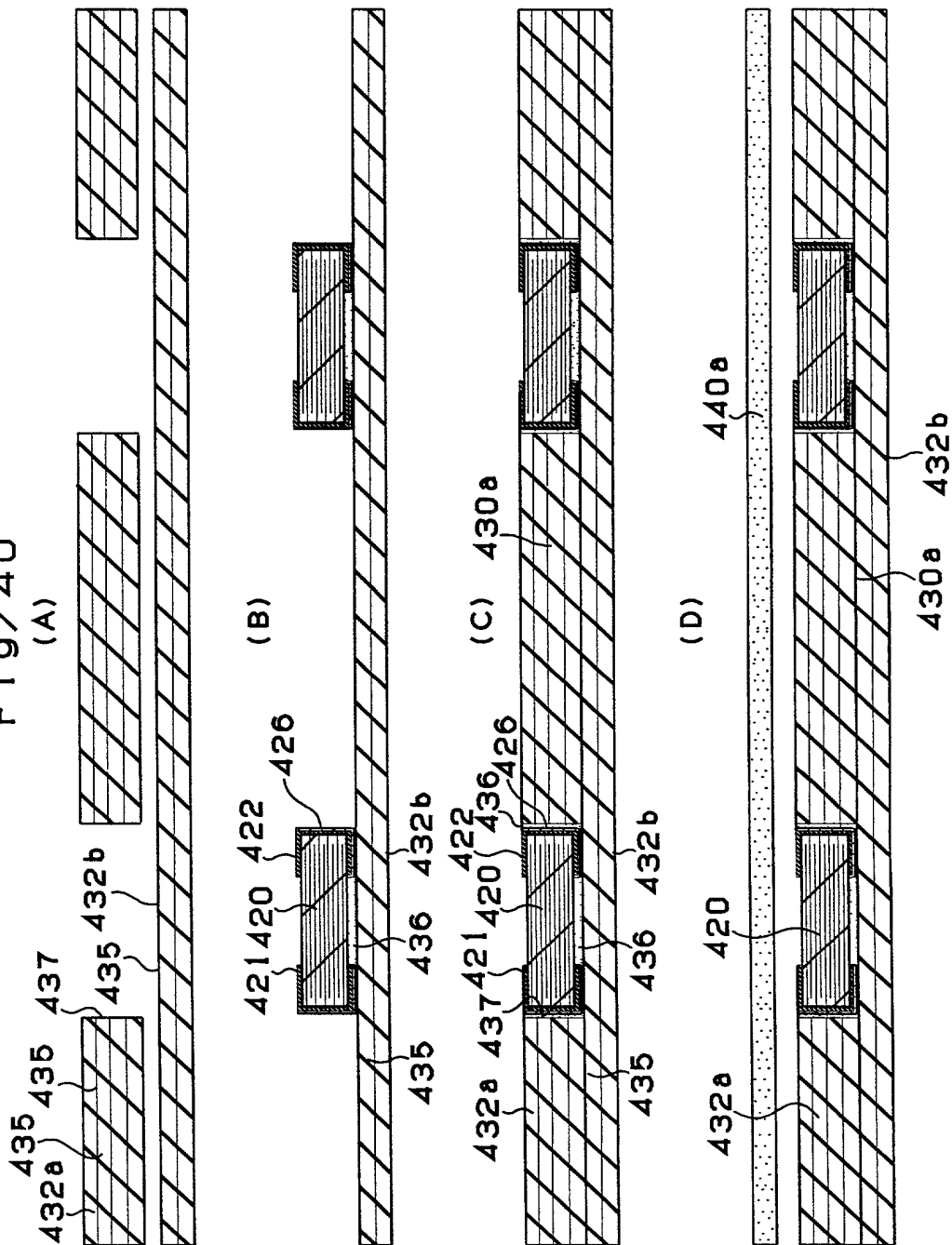
38/73
Fig. 38



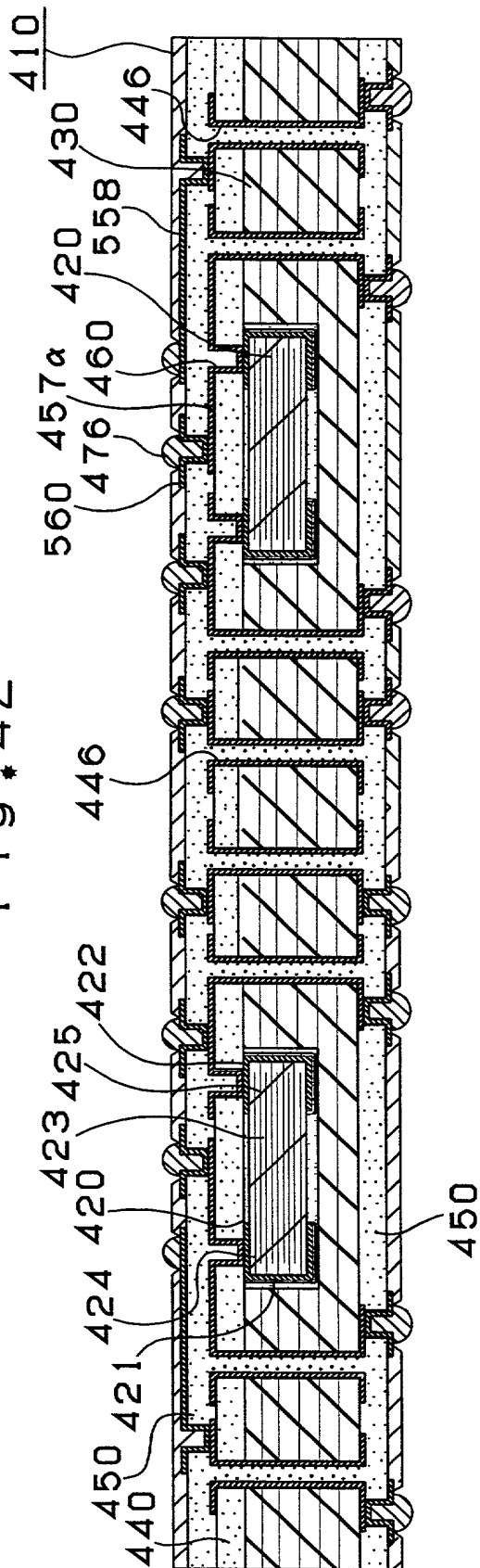
39/73
Fig/39



40/73
Fig/40



42/73
Fig. 42



43/73
Fig. 43

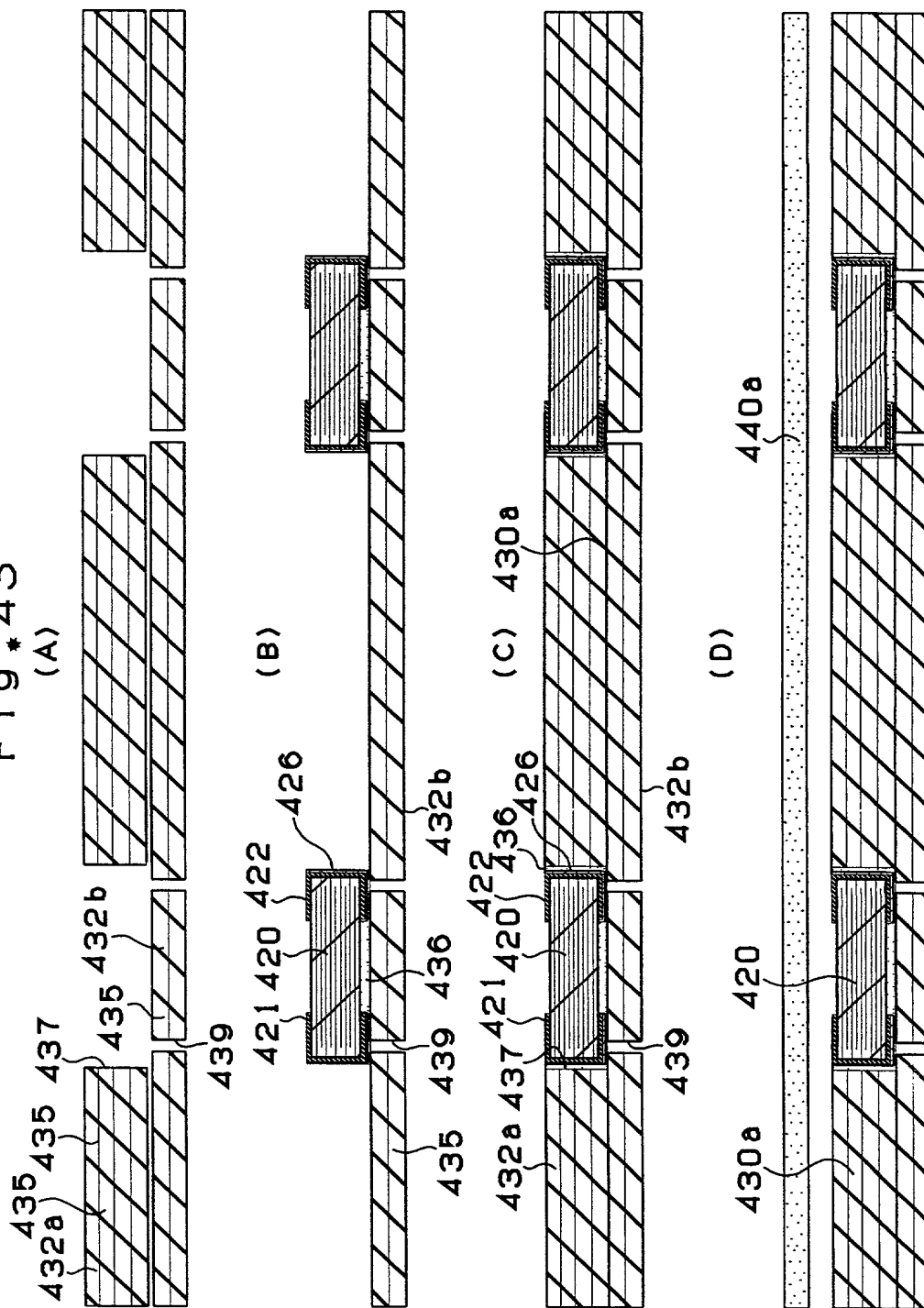
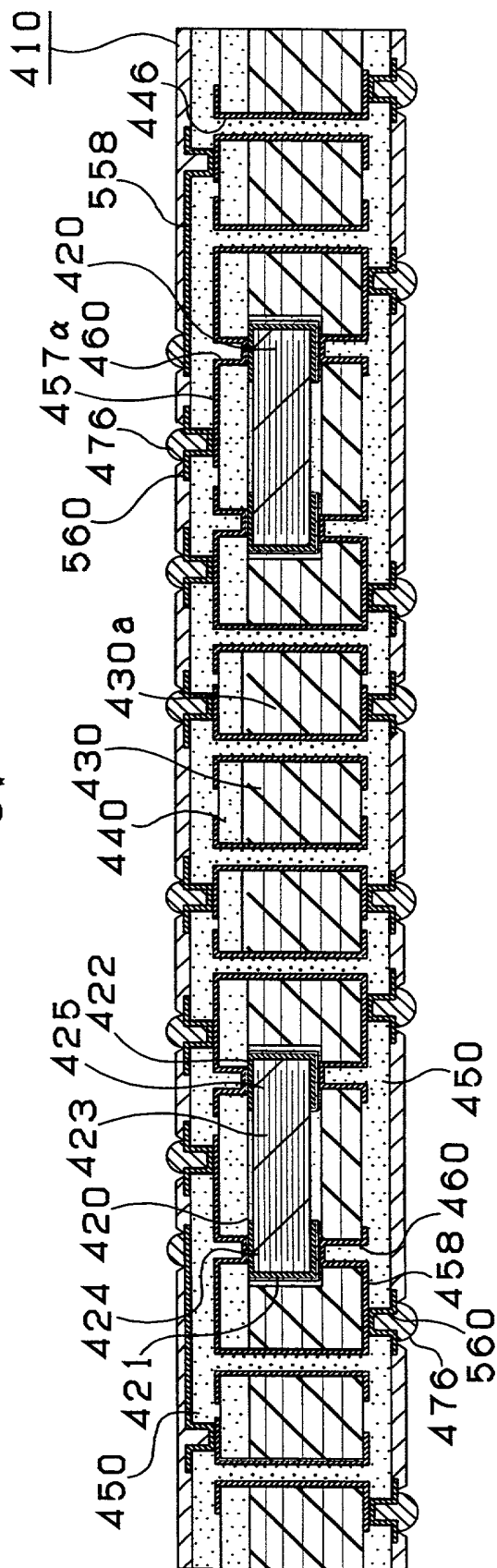
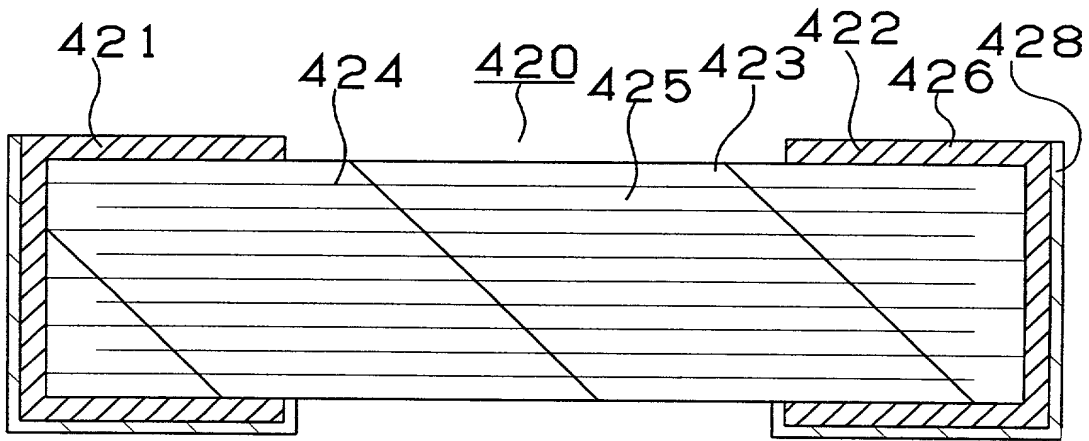


Fig. 44/73*

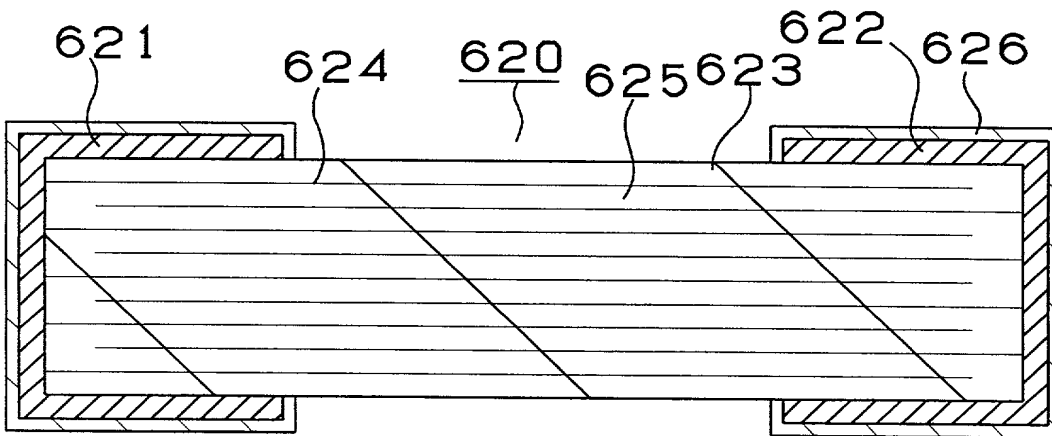


45/73
Fig. 45

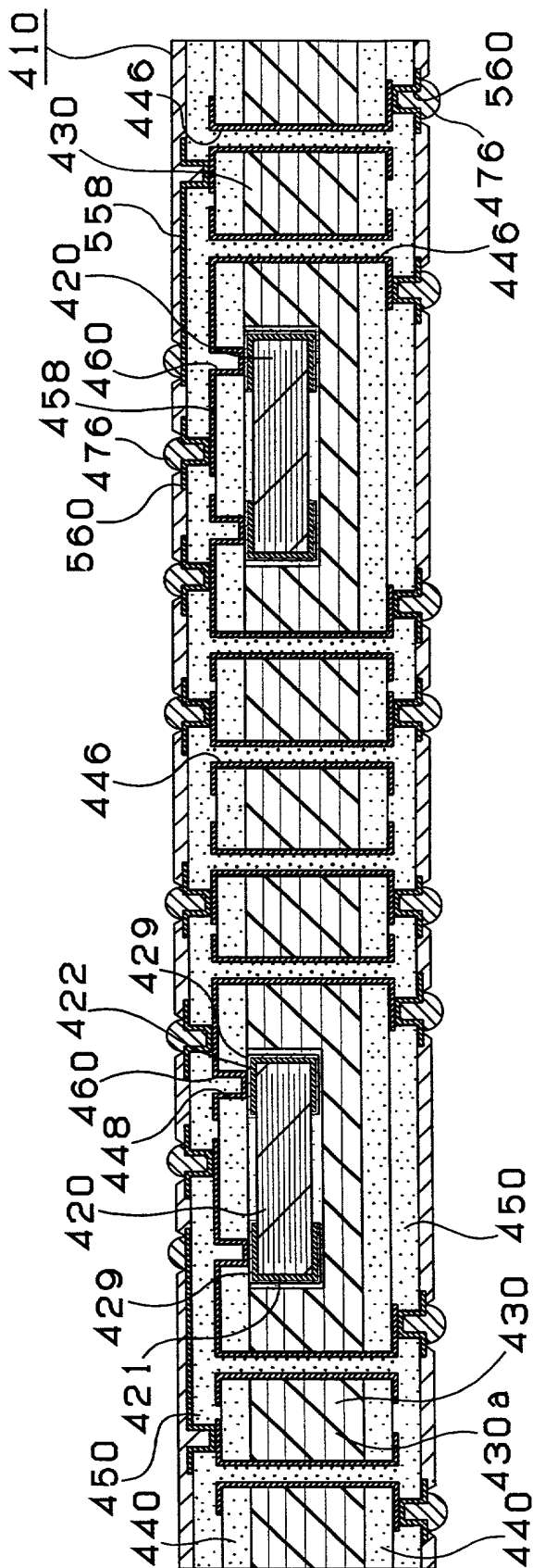
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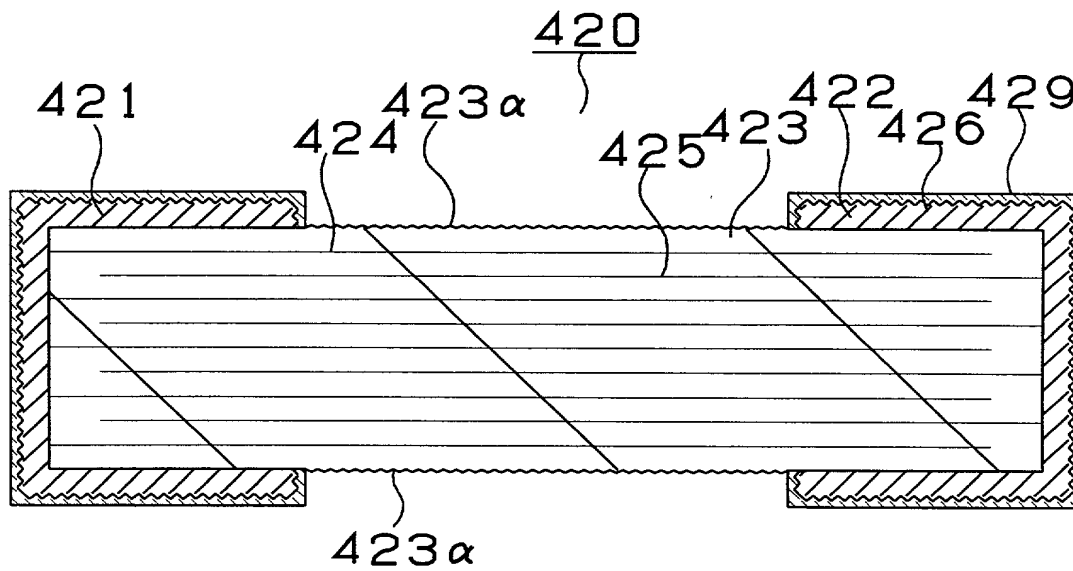


(B)



46/73
Fig. 46



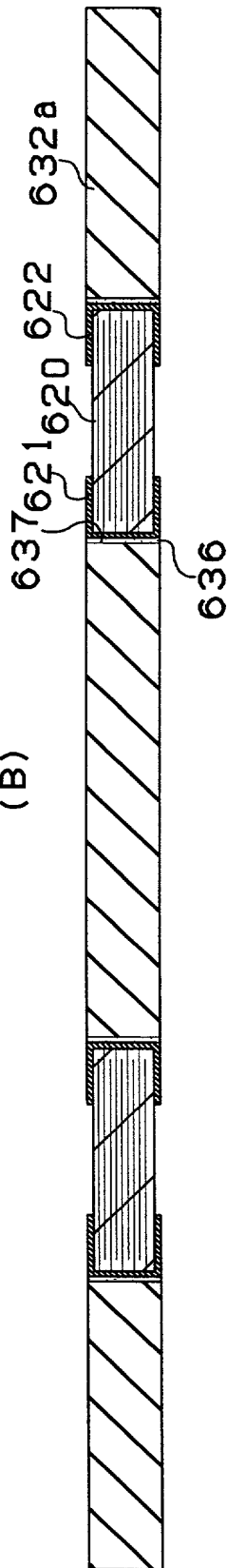
47/73
Fig. 47

48/73
Fig. 48

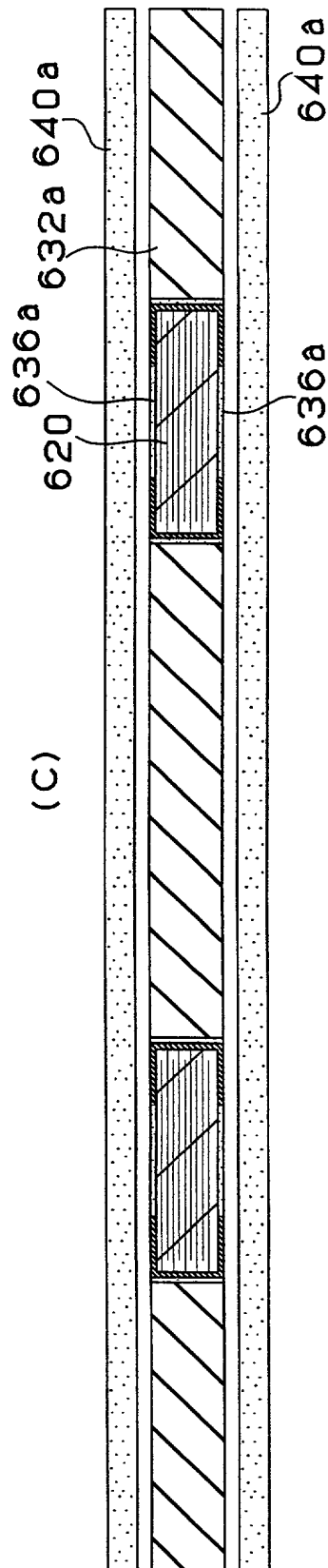
(A)



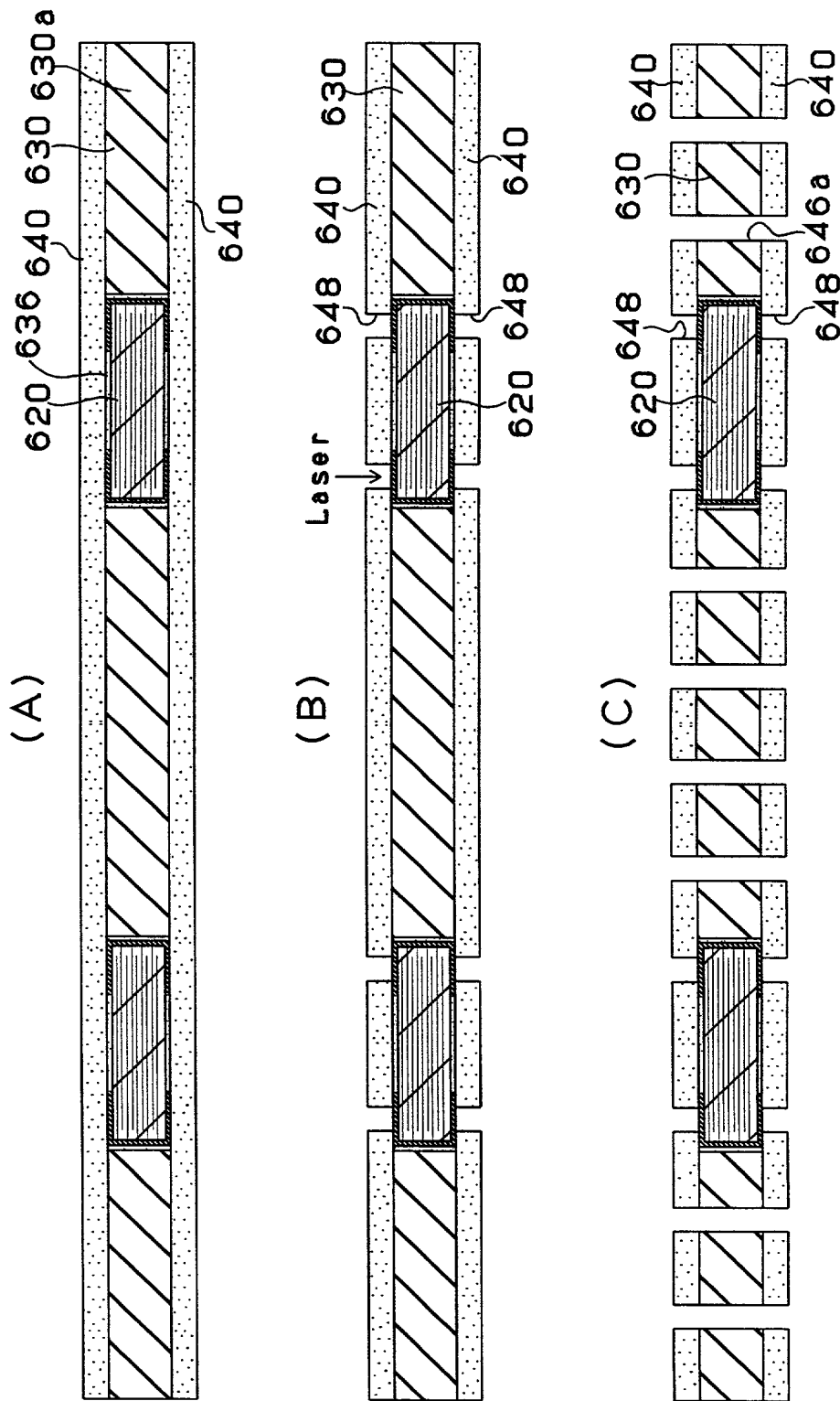
(B)



(C)

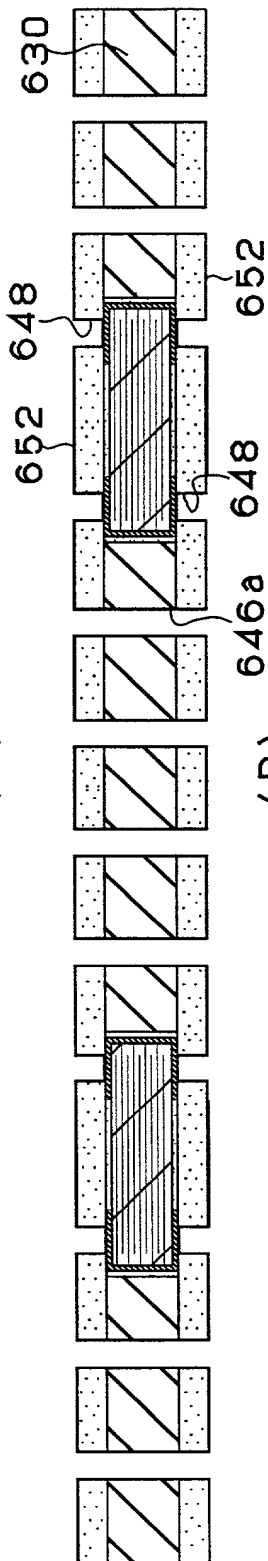


49/73
Fig. 49

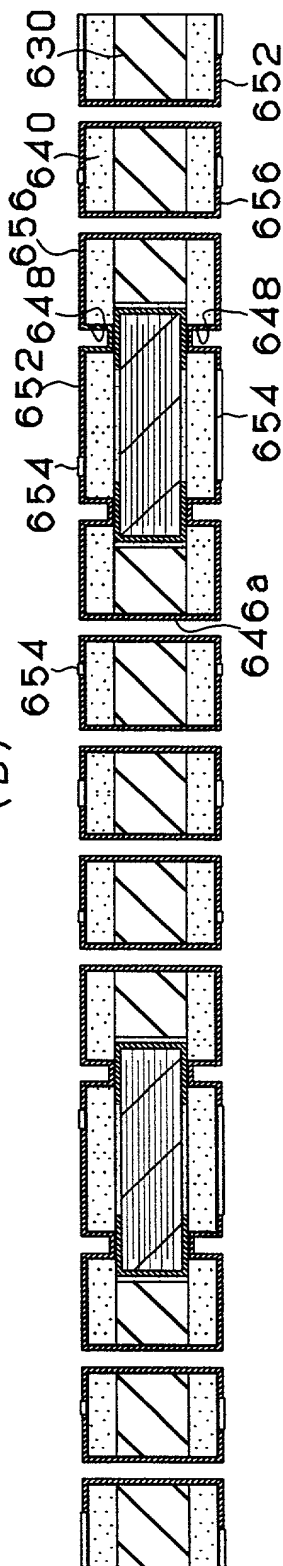


50/73
Fig. 50

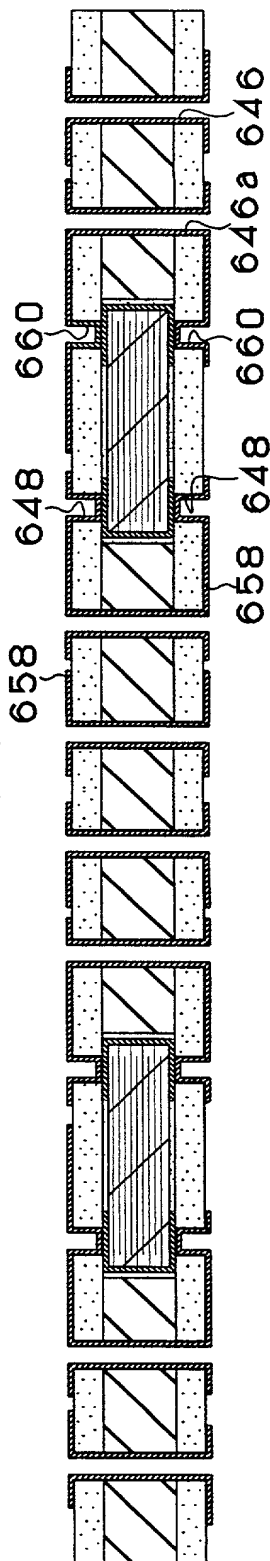
(A)



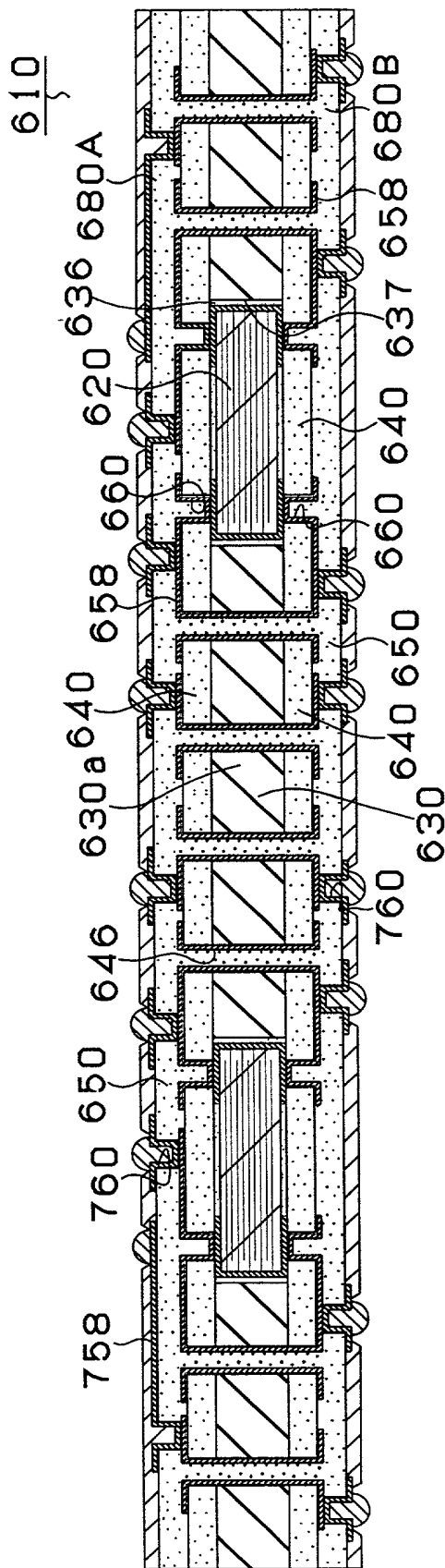
(B)



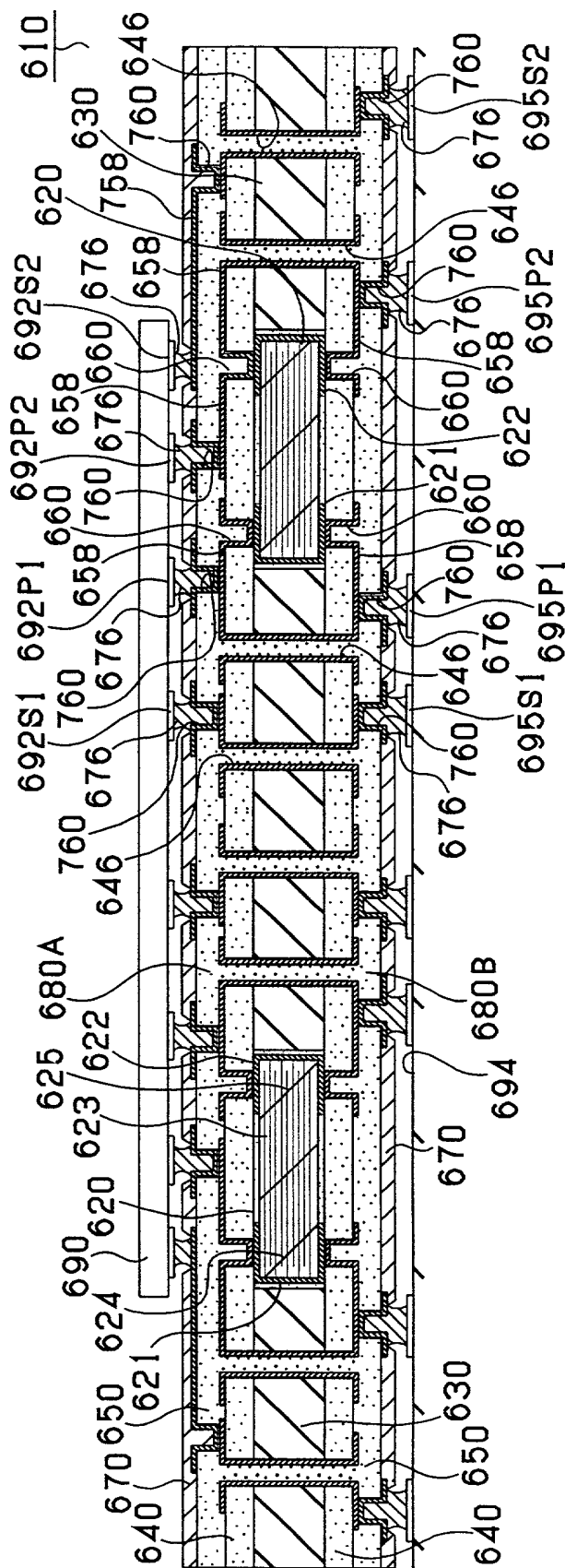
(C)



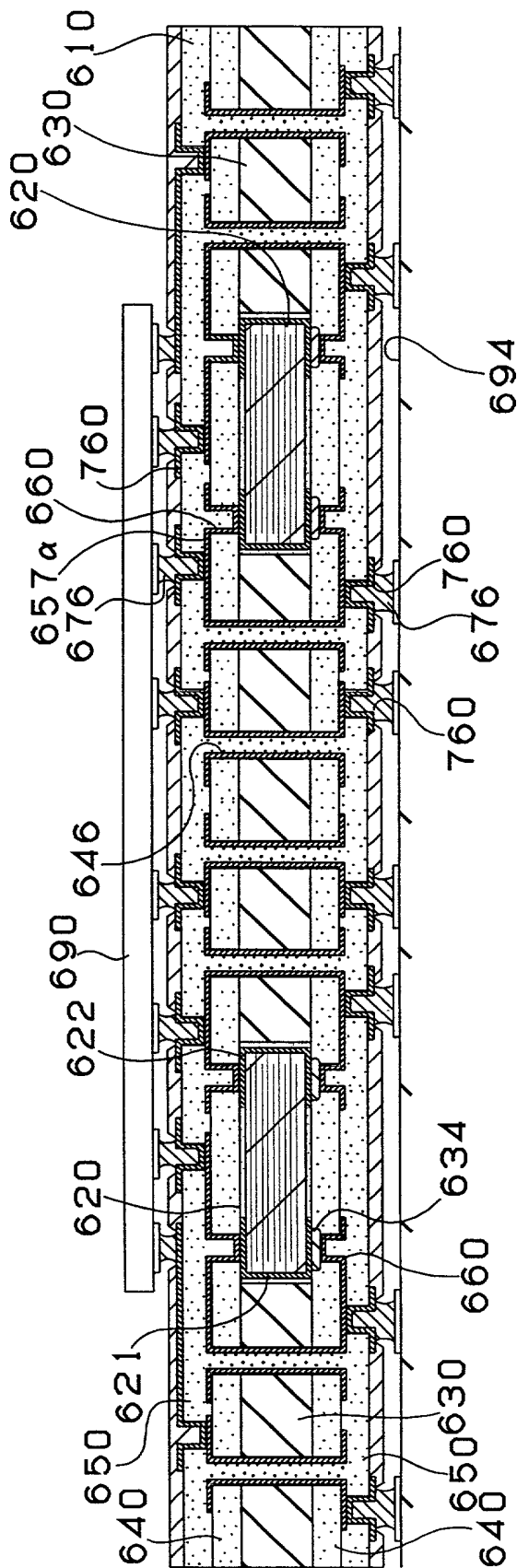
51/73
Fig. 51

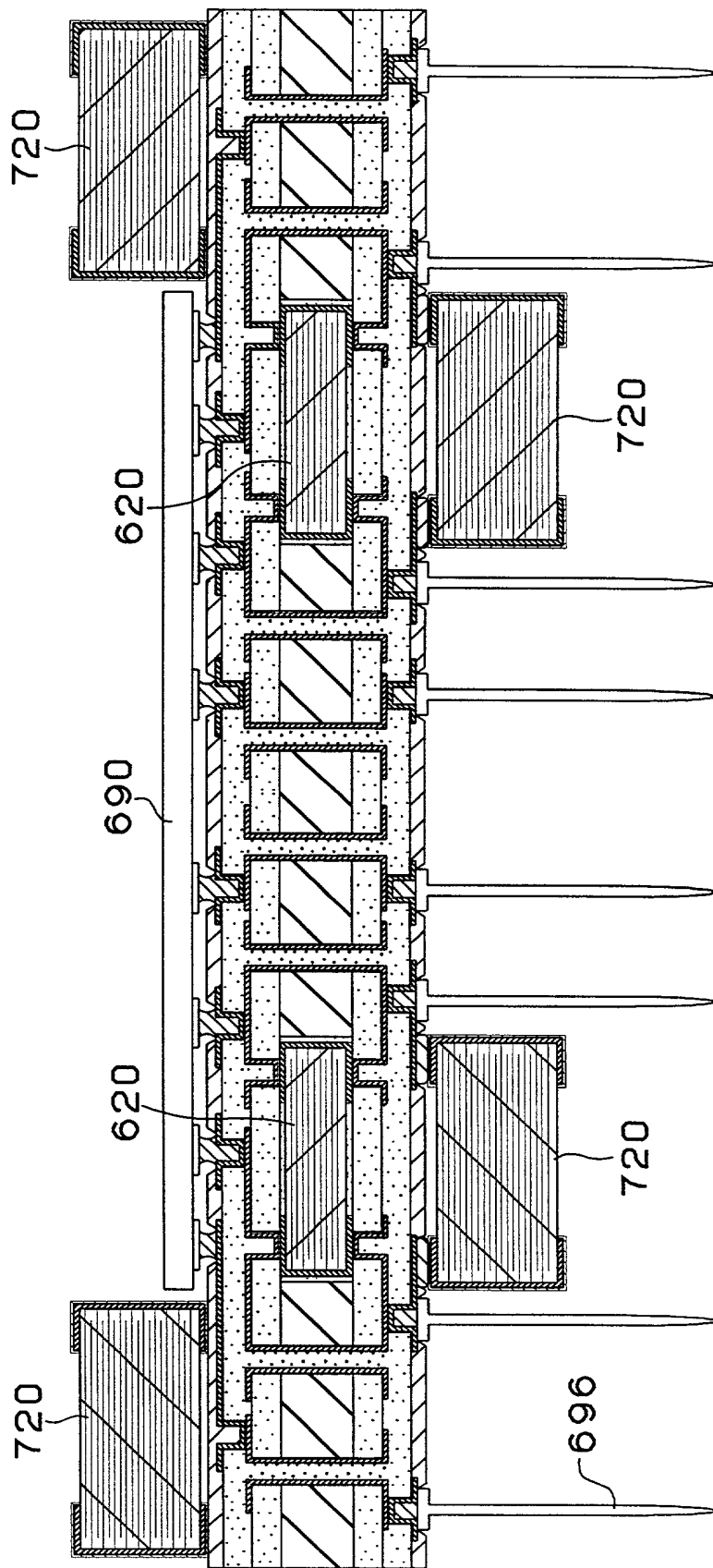


52/73
Fig. 52

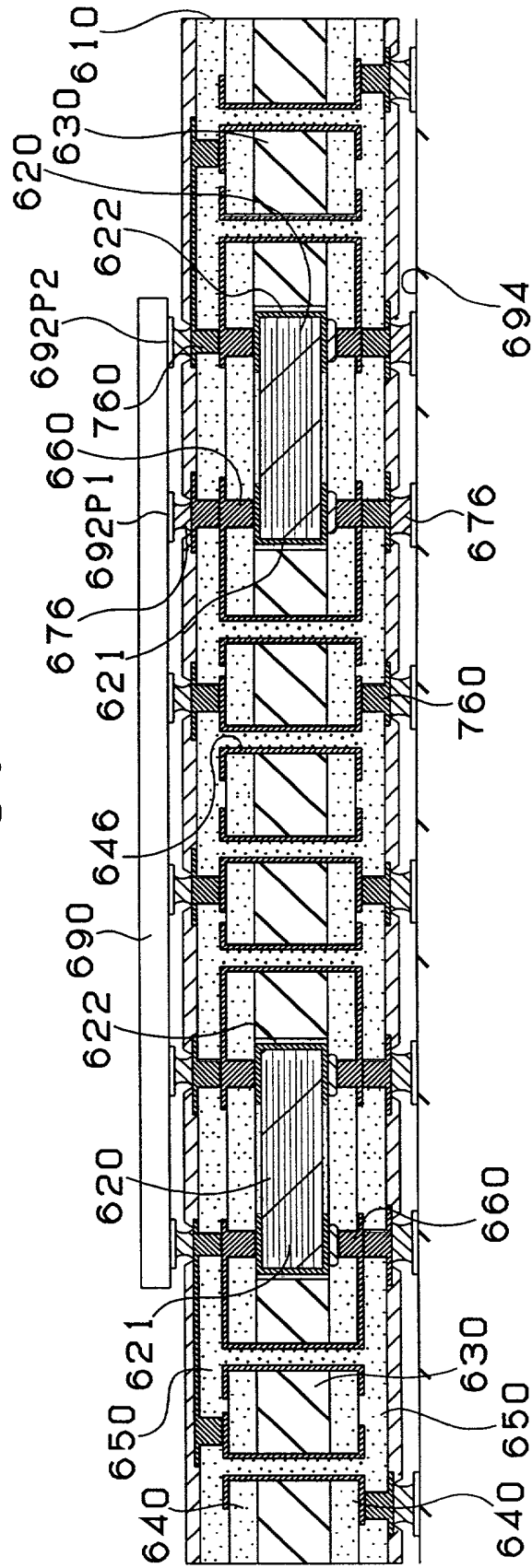


53/73
Fig. 53

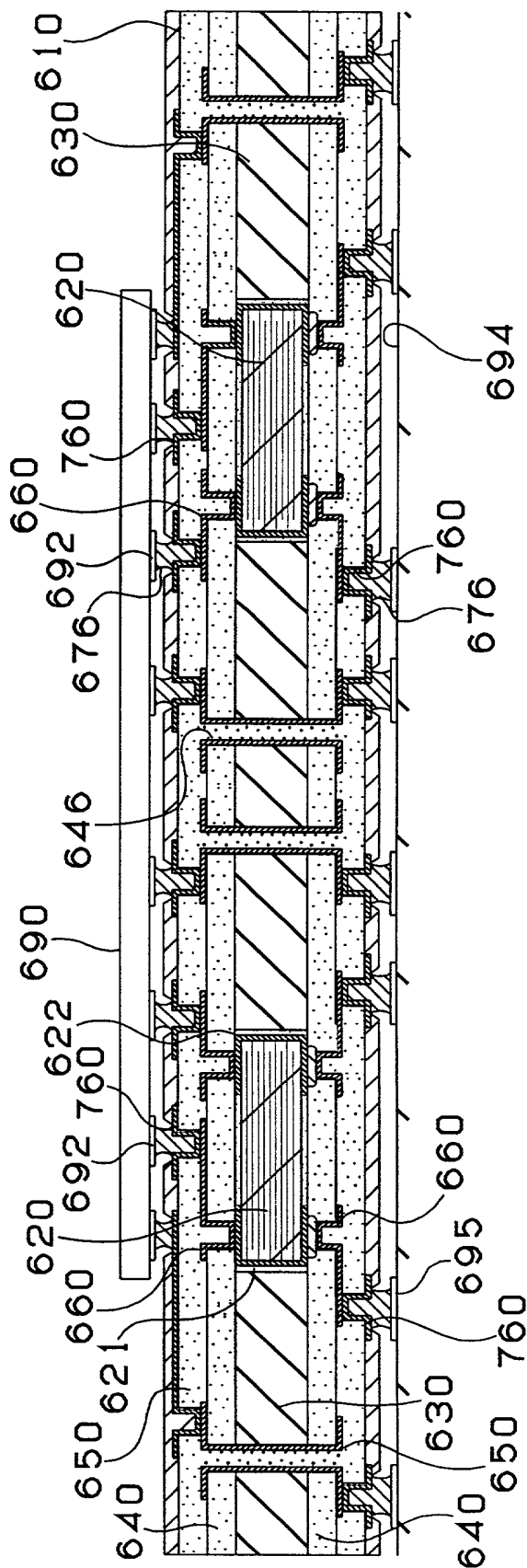




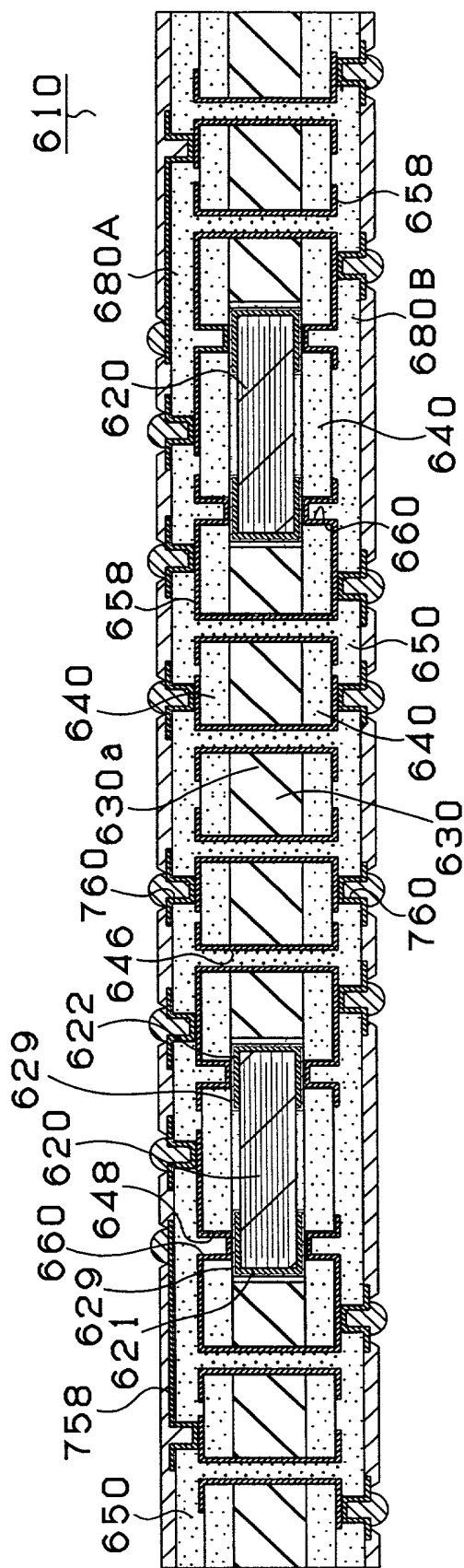
56/73
Fig. 56

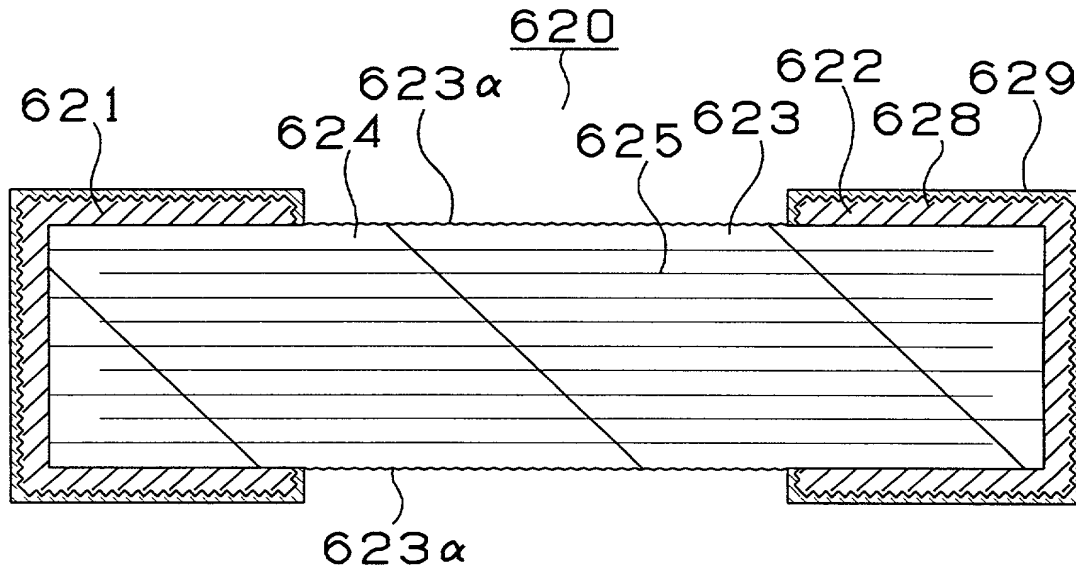


57/73
Fig. 57

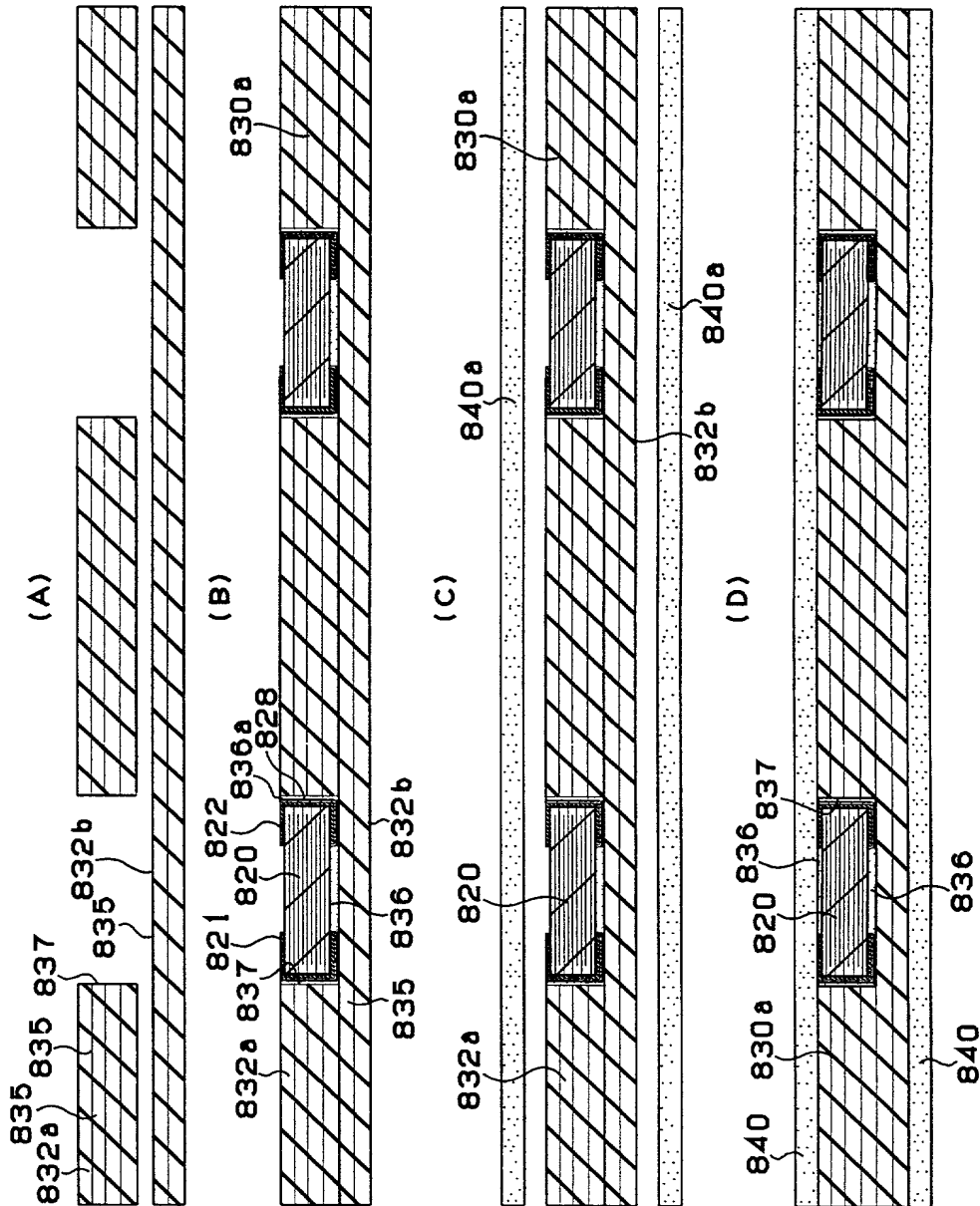


58/73
Fig. 58

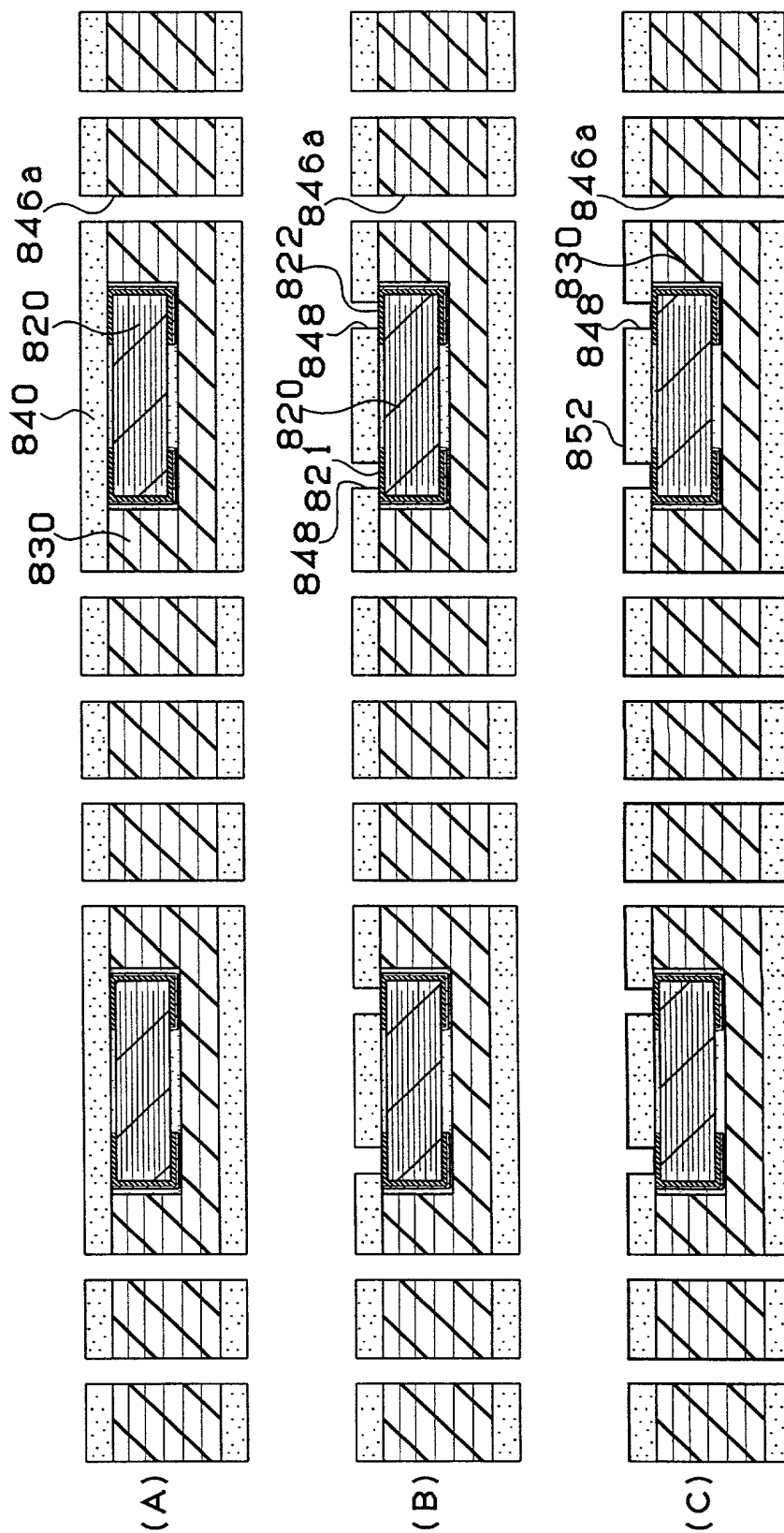


59/73
Fig. 59

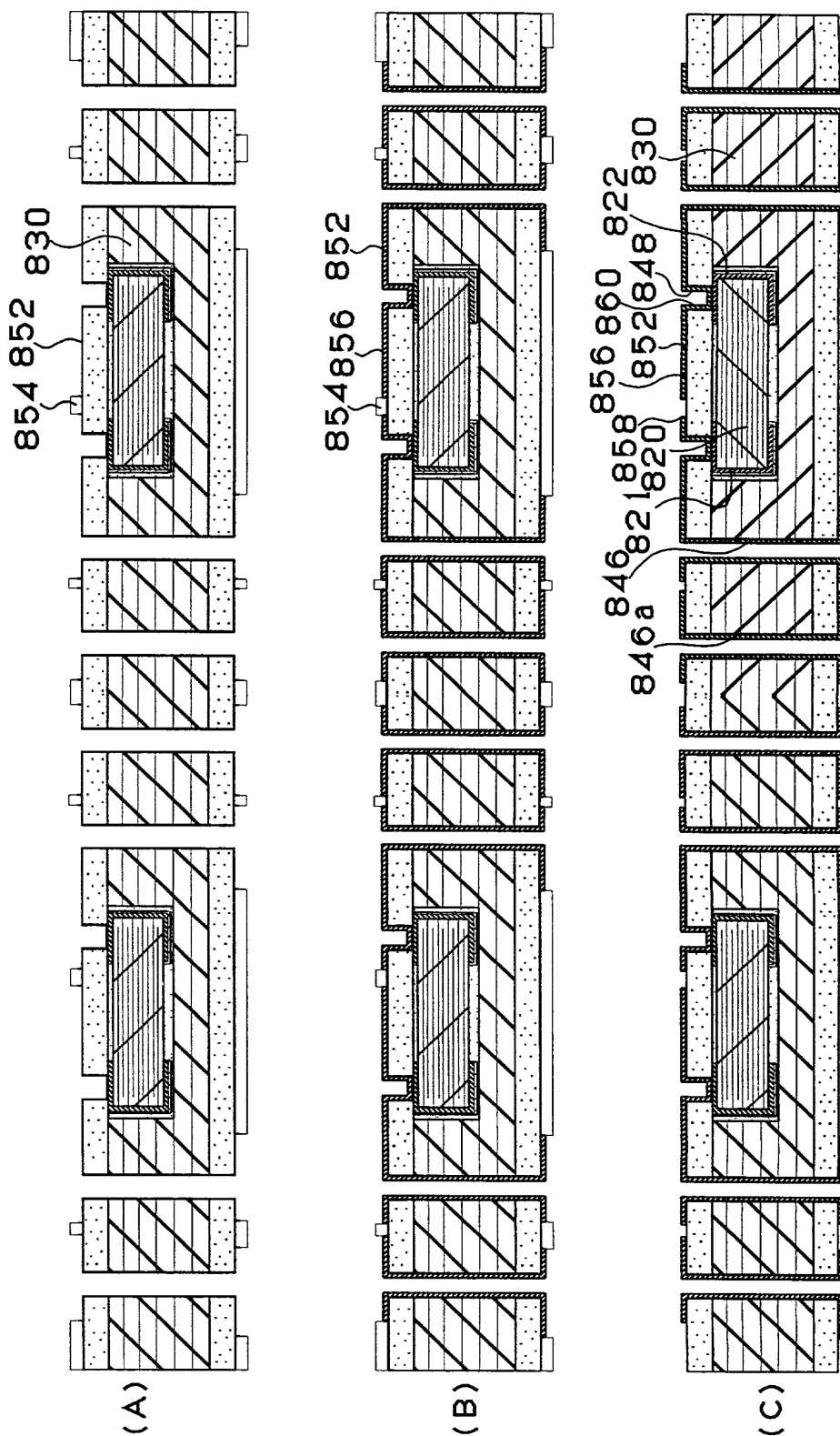
60/73
Fig. 60



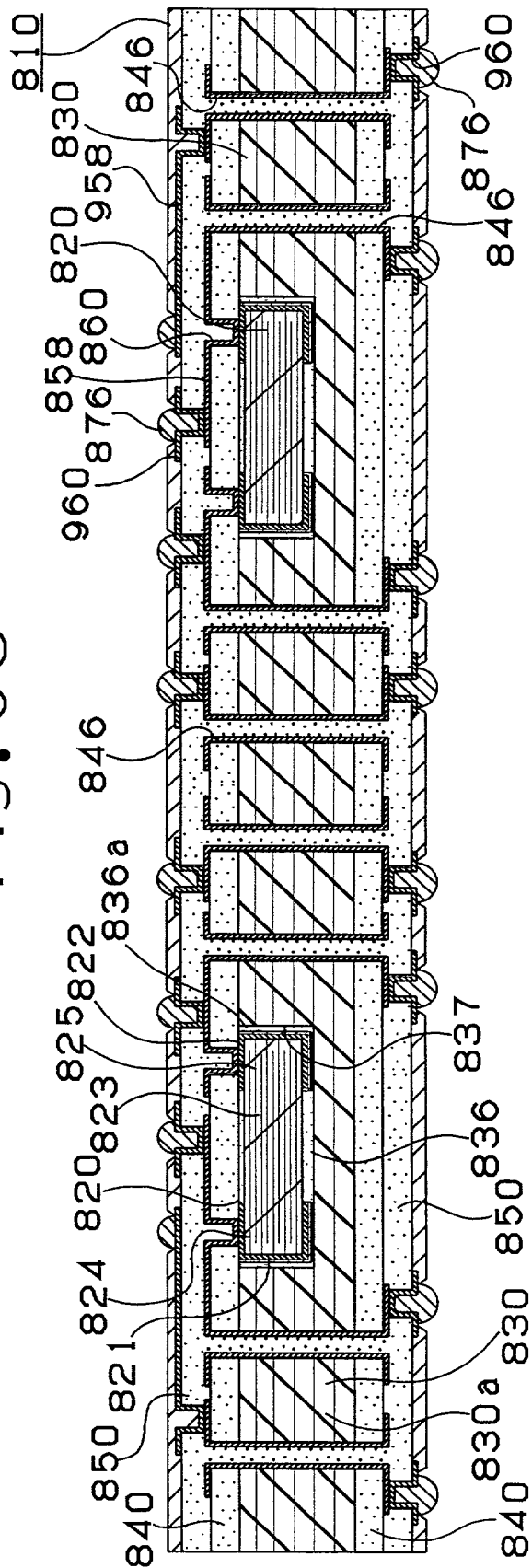
61/73
Fig. 61



62/73
Fig. 62

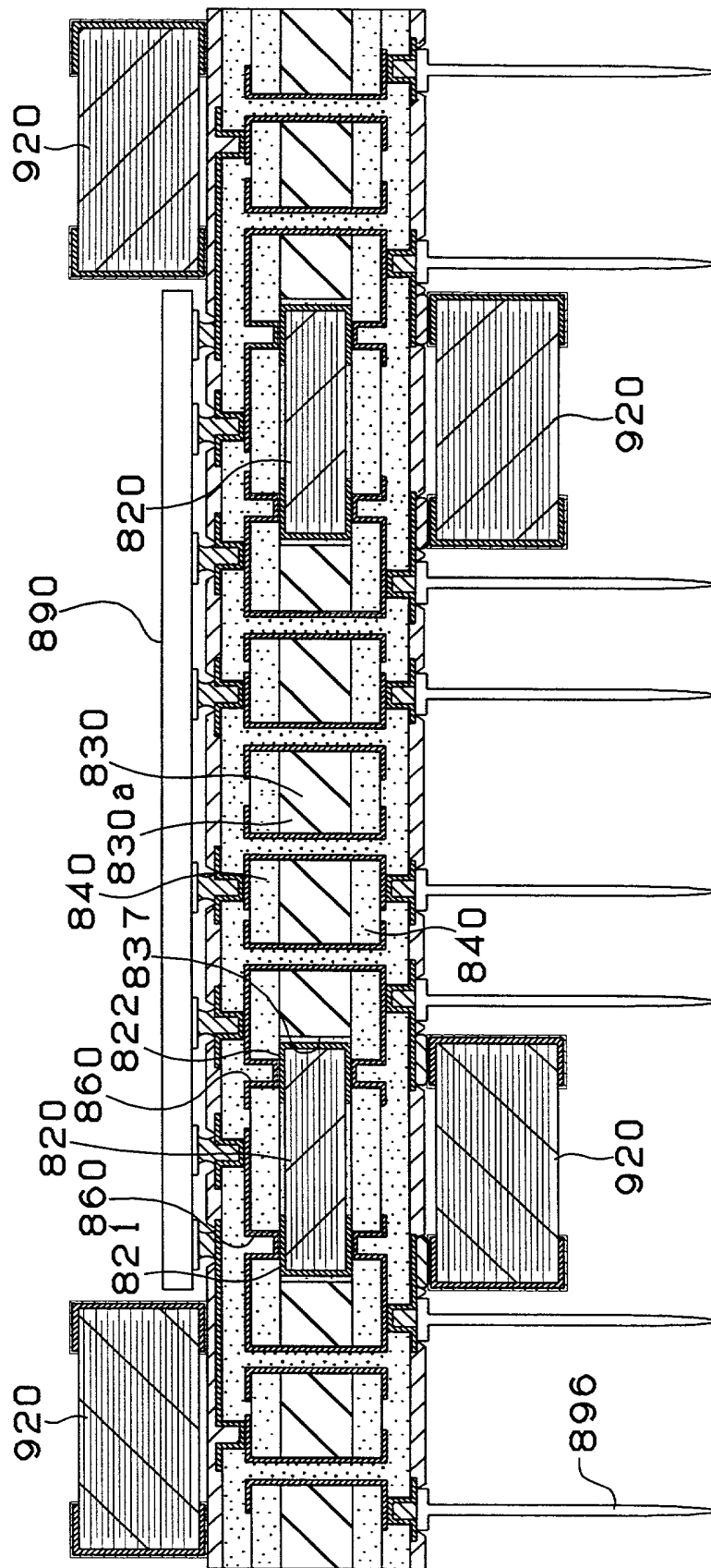


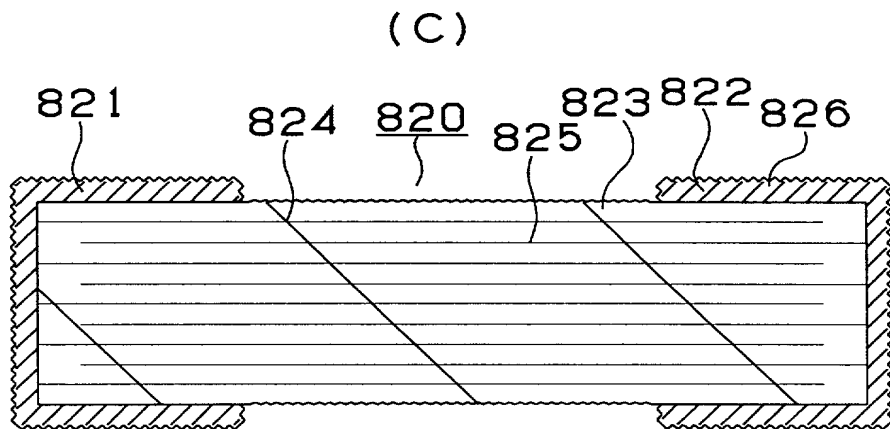
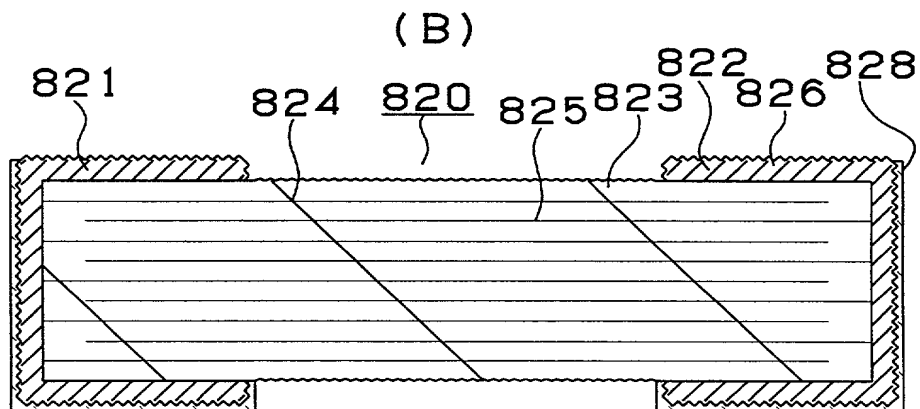
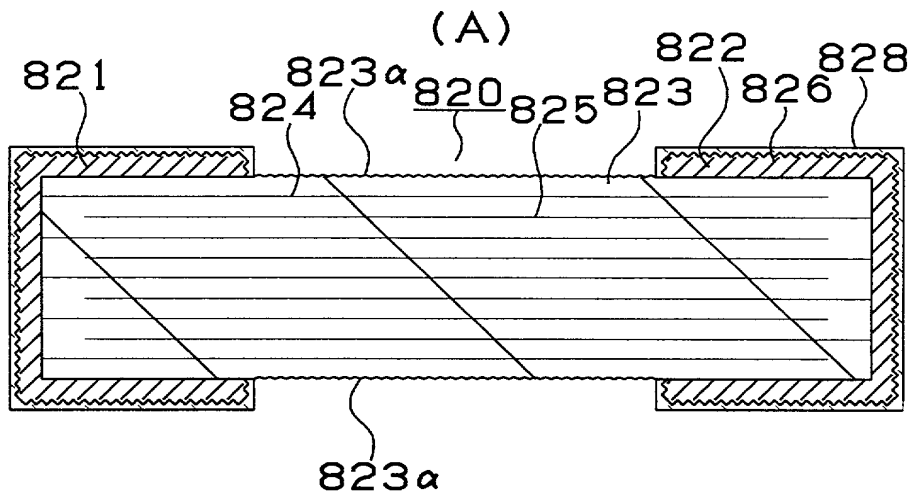
63/73
Fig. 63



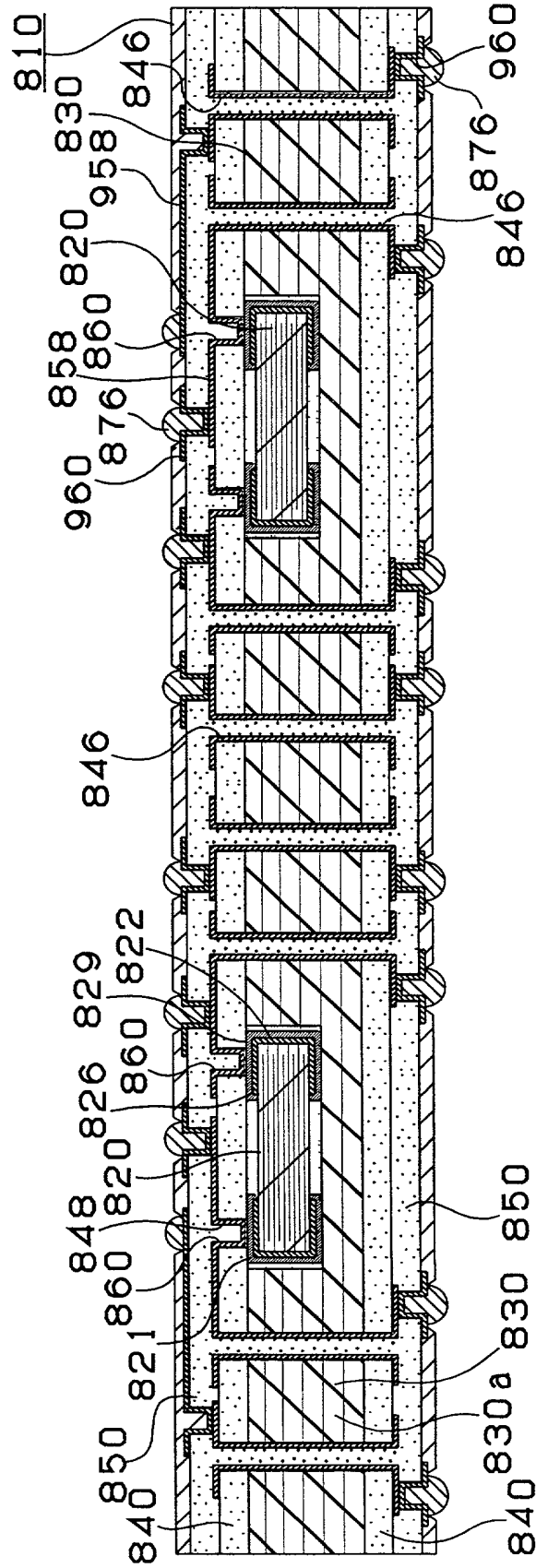
This cross-sectional view illustrates a multi-layered semiconductor device. The structure includes a substrate 840 at the bottom, with a series of layers 820, 821, 822, 823, and 825 stacked on top. A central layer 824 is also present. The device features a series of vertical structures 830, 846, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000. The device is shown in a cross-sectional view, with various layers and components labeled with reference numerals.

65/73
Fig. 65



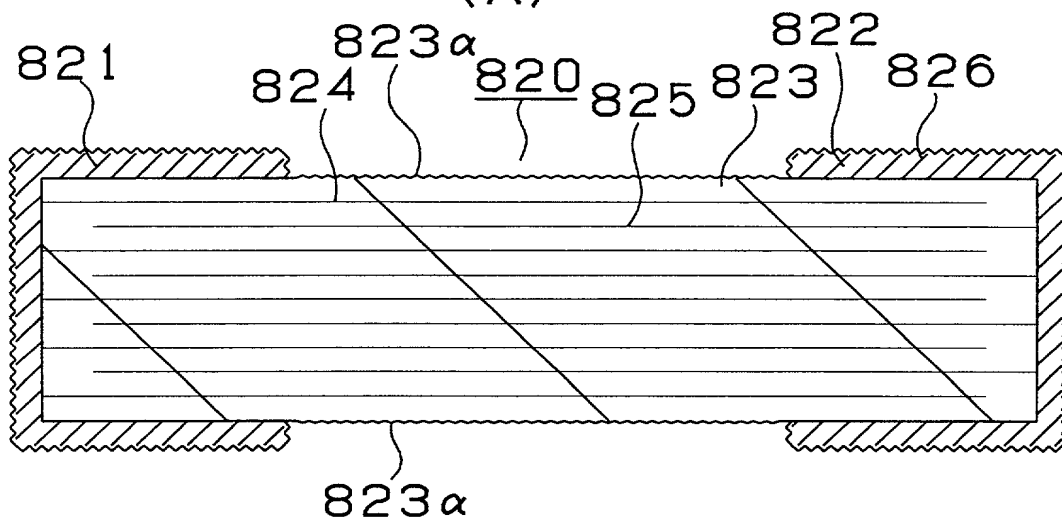
66/73
Fig. 66

67/73
Fig. 67

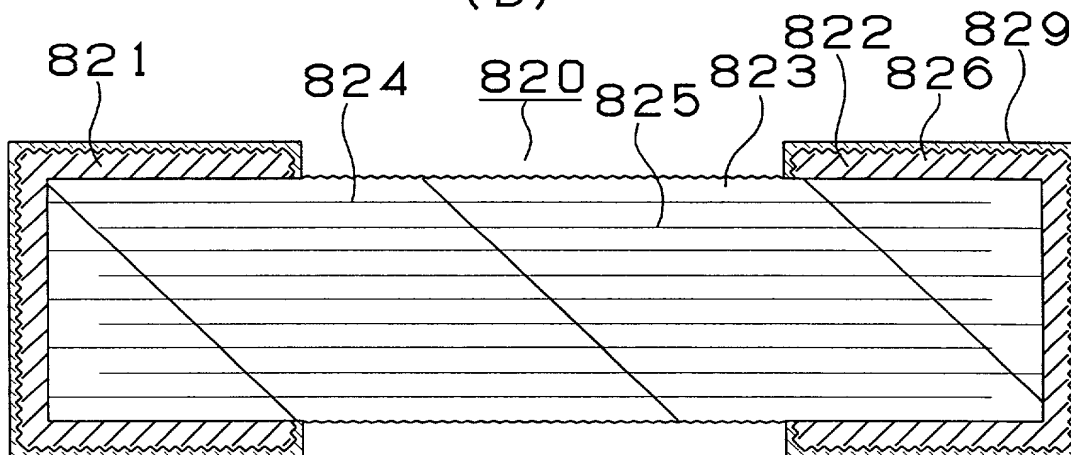


68/73
Fig. 68

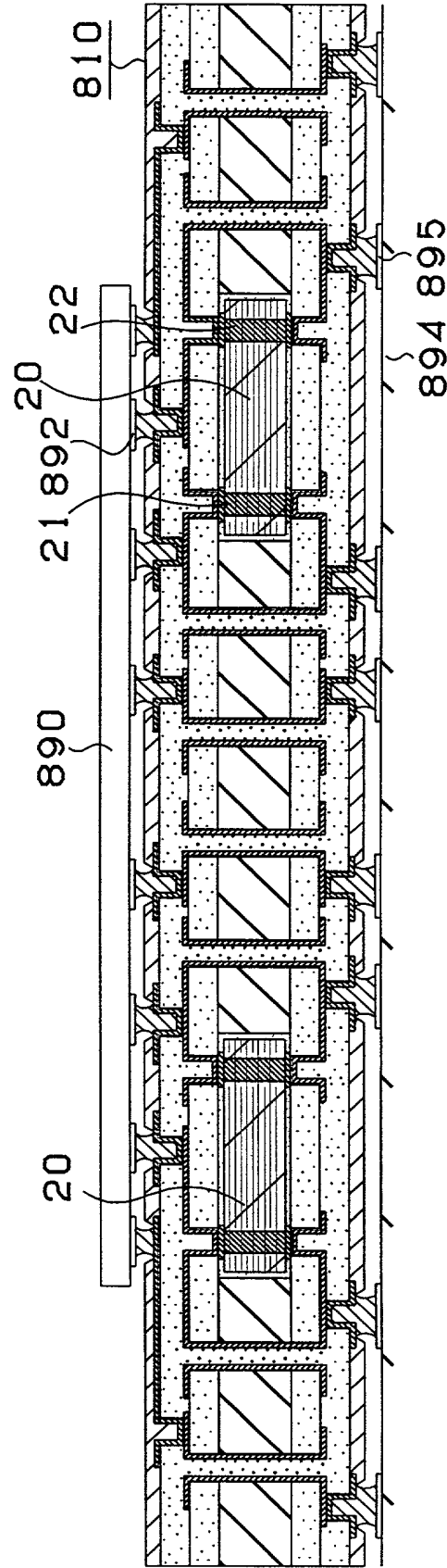
(A)



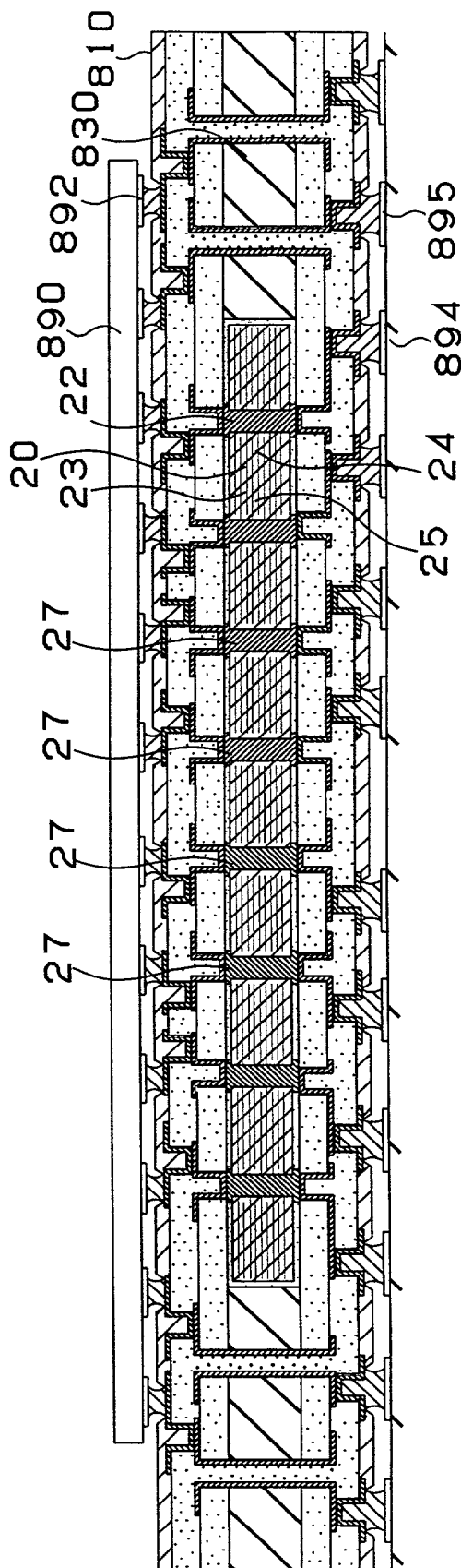
(B)



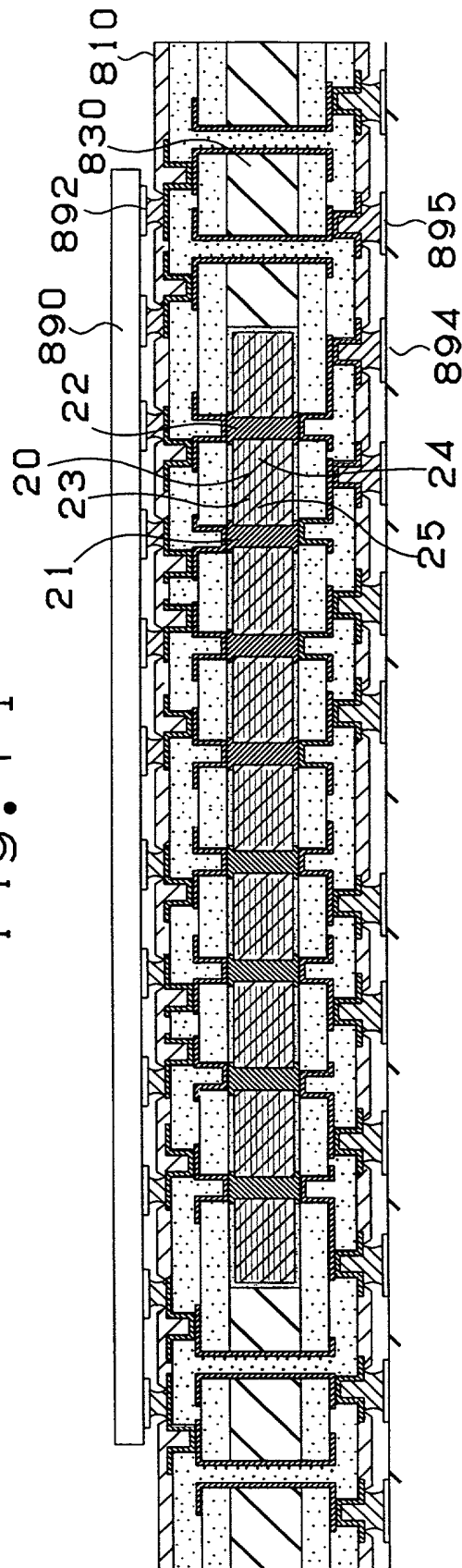
69/73
Fig. 69



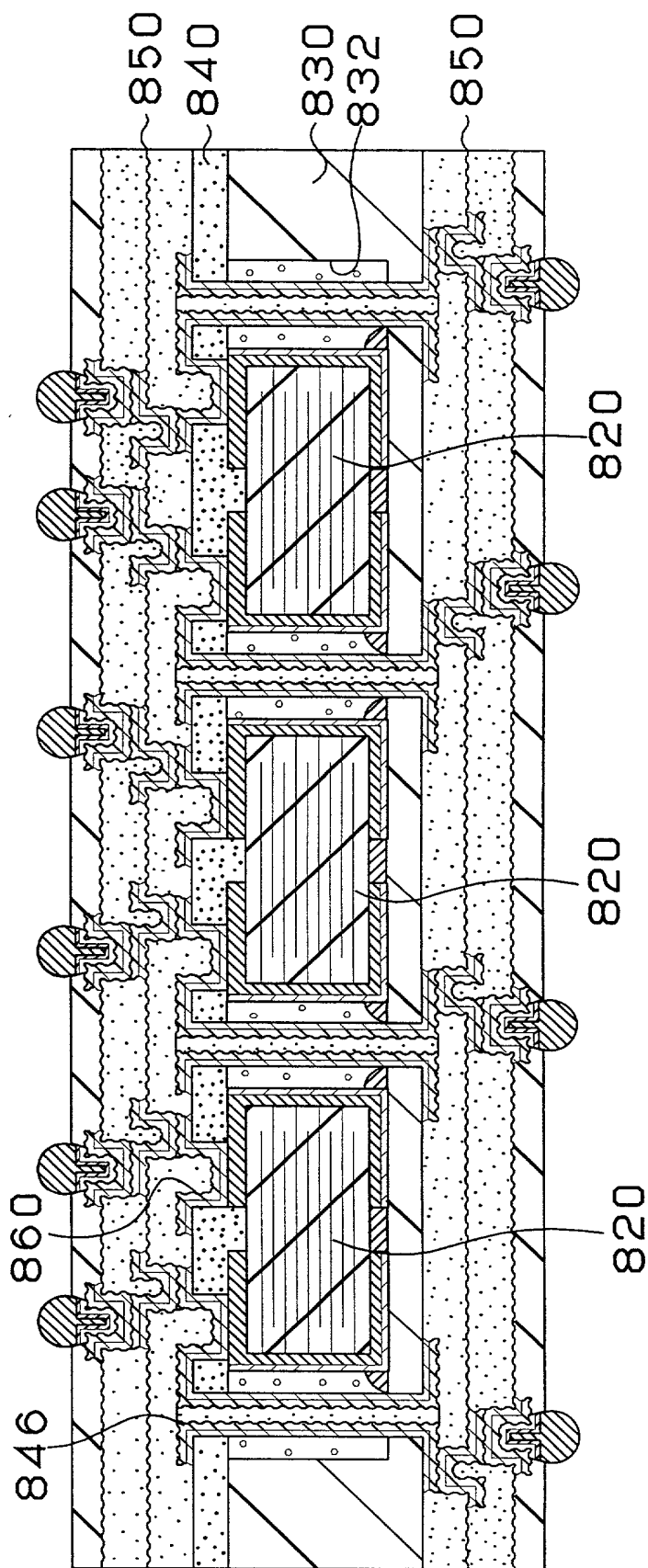
70/73
Fig. 70



71/73
Fig. 71

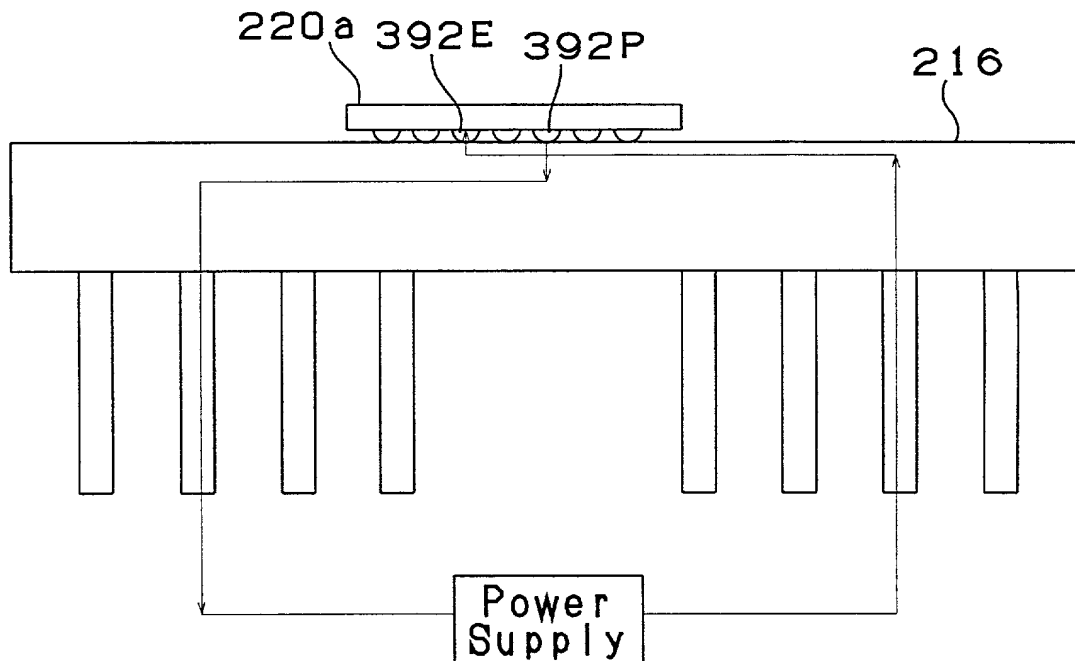


72/73
Fig. 72

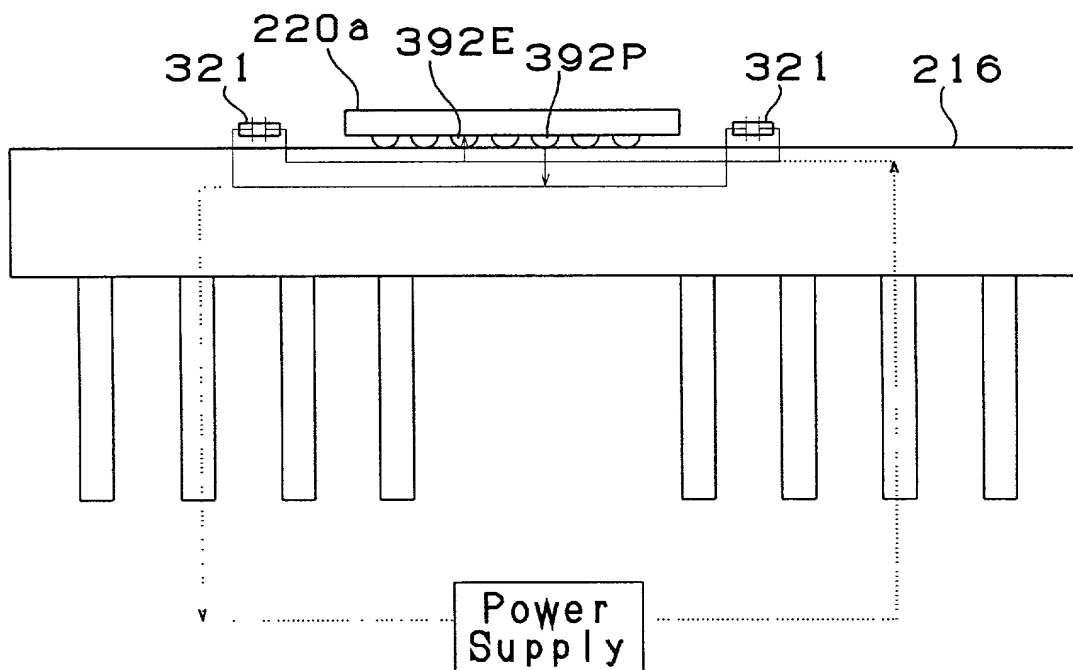


73/73
Fig. 73

(A)



(B)



FOR UTILITY/DESIGN
CIP/PCT NATIONAL/PLANT
ORIGINAL/SUBSTITUTE/SUPPLEMENTAL
DECLARATIONS

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Pillsbury
Winthrop
FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the **INVENTION ENTITLED**

Printed Circuit Board And Method For Manufacturing Printed Circuit Board

the specification of which (CHECK applicable BOX(ES))

X A. ☐ is attached hereto.
BOX(ES) → B. ☐ was filed on _____ as U.S. Application No. _____ /
→ C. ☒ was filed as PCT International Application No. PCT/ JP00/05972 on September 1, 2000

and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. Except as noted below, I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application.

PRIOR FOREIGN APPLICATION(S)

Number	Country	Day/MONTH/Year Filed	Date first Laid-open or Published	Date Patented or Granted	Priority NOT Claimed
11-248311	Japan	2/September/1999			
11-360306	Japan	20/December/1999			
2000-103730	Japan	5/April/2000			
2000-103731	Japan	5/April/2000			
2000-103732	Japan	5/April/2000			
2000-103733	Japan	5/April/2000			

If more prior foreign applications, X box at bottom and continue on attached page.

Except as noted below, I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S)

Application No. (series code/serial no.)	Day/MONTH/Year Filed	Status	Priority NOT Claimed
		pending, abandoned, patented	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Winthrop LLP, Intellectual Property Group, 1100 New York Avenue, N.W., Ninth Floor, East Tower, Washington, D.C. 20005-3918, telephone number (202) 861-3000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

Paul N. Kokulis	16773	Glenn J. Perry	28458	Stephen C. Glazier	31361	William P. Atkins	38824
Kevin E. Joyce	20508	G. Paul Edgell	24238	Richard H. Zaitlen	27248	Paul L. Sharer	36004
George M. Sirilla	18224	Lynn E. Eccleston	35861	Roger R. Wise	31204	Robin L. Teskin	35030
Donald J. Bird	25323			Michael R. Dzwonczyk	36787		
		David A. Jakopin	32995	W. Patrick Bengtsson	32456		
Dale S. Lazar	28872	Mark G. Paulson	30793	Jack S. Barufka	37087		
				Adam R. Hess	41835		

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(include Zip Code)	501-0695	

"X" box ☒ FOR ADDITIONAL INVENTORS, and proceed on the attached page to list each additional inventor.

☒ See additional foreign priorities on attached page (incorporated herein by reference).

Atty. Dkt. No. PM

(M#)

DECLARATION AND POWER OF ATTORNEY

(continued)

ADDITIONAL INVENTORS:

(3) INVENTOR'S SIGNATURE:

Date:

3/22/2001

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First	Middle Initial	Family Name	
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(include Zip Code)	501-0695		

(4) INVENTOR'S SIGNATURE:

Date:

3/22/2001

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(include Zip Code)	501-0695		

(5) INVENTOR'S SIGNATURE:

Date:

3/22/2001

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City	State/Foreign Country		Country of Citizenship
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(include Zip Code)	501-0695		

RULE 63 DECLARATION AND POWER OF ATTORNEY

(continued)

ADDITIONAL PRIOR FOREIGN APPLICATIONS

<u>PRIOR FOREIGN APPLICATION(S)</u>		<u>Date/MONTH/Year</u>	<u>Date first Laid-open or</u>	<u>Date Patented or</u>		<u>Priority NOT</u>
<u>Number</u>	<u>Country</u>	<u>Filed</u>	<u>Published</u>	<u>Granted</u>		<u>Claimed</u>
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2000-221351	Japan	21/July/2000				<input type="checkbox"/>
2000-221352	Japan	21/July/2000				<input type="checkbox"/>
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